SSD1320

Product Preview

160 x 160, 16 Gray Scale Dot Matrix OLED/PLED Segment/Common Driver with Controller

Appendix: IC Revision history of SSD1320 Specification

Version	Change Items	Effective Date
0.10	1st Release	21-Feb-17

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FIGURES

1 GENERAL DESCRIPTION

SSD1320 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display. It consists of 160 segments and 160 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1320 embeds with contrast control, display RAM and oscillator, which reduce the number of external components and power consumption. It has 160 x 160 x 4 bits Graphic Display Data RAM (GDDRAM), and supports 256-step contrast. Data/Commands are sent from generic MCU through the hardware selectable 6800/8080 series compatible Parallel Interface, I2C interface or Serial Peripheral Interface. SSD1320 is designed to support high brightness panel, with maximum source current reaching 600uA, making it suitable for many compact portable applications which requires sunlight readability, such as wearable electronics etc.

2 FEATURES

- Resolution: 160 x 160 dot matrix panel
- Power supply
  - V_{DD} = 1.65V – 3.5V (for IC logic)
  - V_{CC} = 8.0V – 18.0V (for Panel driving)
- Segment maximum source current: 600uA
- Common maximum sink current: 96mA
- Embedded 160 x 160 x 4 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8 bits 6800/8080-series parallel Interface
  - 3/4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Screen saving infinite content scrolling function
- Internal or external I_{REF} selection
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- Power On Reset (POR)
- On-Chip Oscillator
- Power Save Mode
- Chip layout for COG, COF
- Wide range of operating temperature: -40°C to 85°C

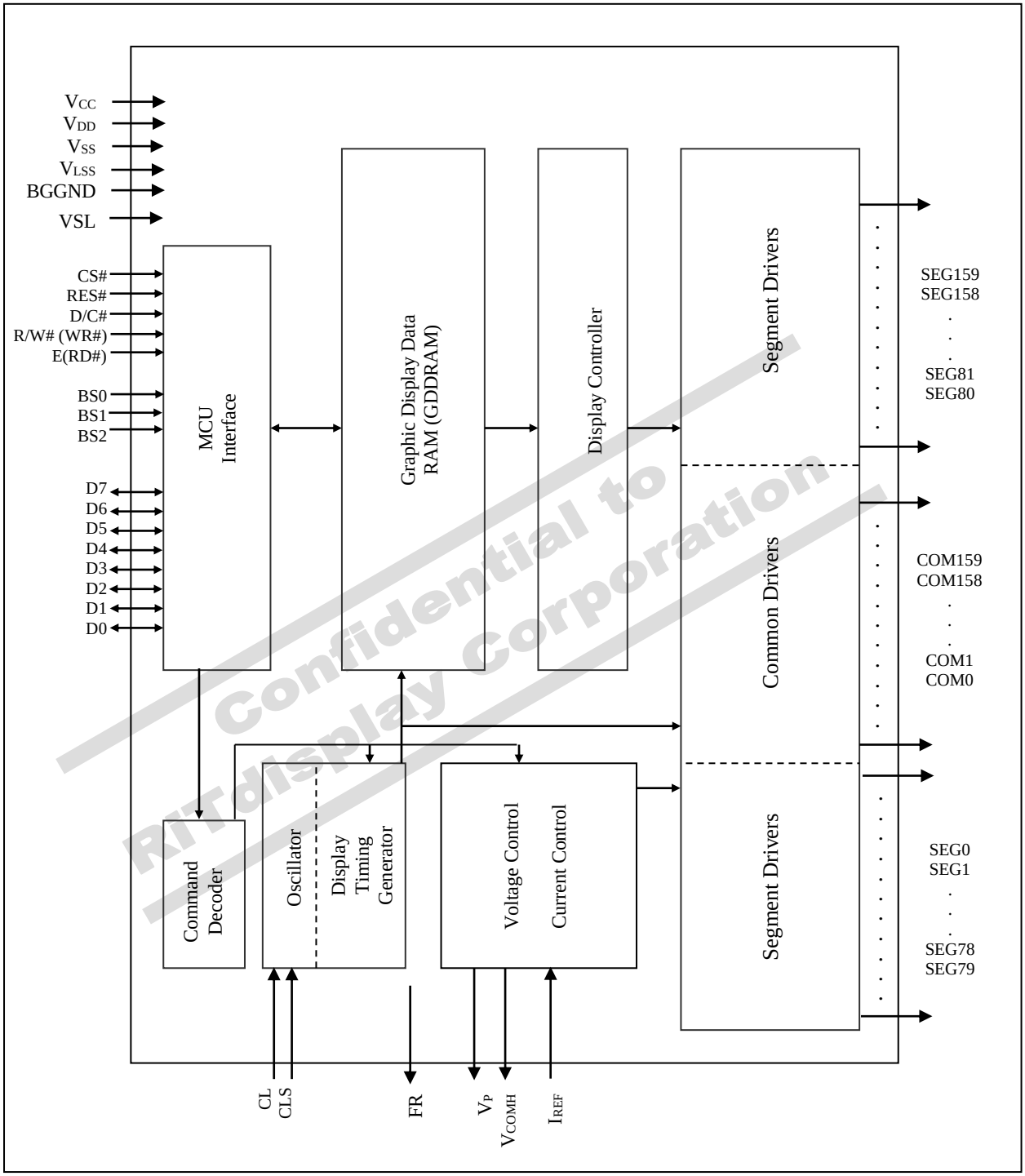
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Remark
SSD1320Z	160	160	COG	○ Min SEG pad pitch : 27um ○ Min COM pad pitch : 27um ○ Min I/O pad pitch : 55um ○ Die thickness: 250um ○ Bump height: nominal 9um

4 BLOCK DIAGRAM

Figure 4-1 –SSD1320 Block Diagram



5 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Table 5-1: Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
BGGND	P	Reserved pin. It must be connected to ground.
V_{SS}	P	Ground pin. It must be connected to external ground.
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.
VSL	P	This is segment voltage (output low level) reference pin. When external VSL is not used, this pin should be connected to V_{LSS} externally. When external VSL is used, this pin should be connected with resistor and diode to ground (details depends on application).
V_{LH}	P	Logic high (same voltage level as V_{DD}) for internal connection of input and I/O pins. No need to connect to external power source.
V_{LL}	P	Logic low (same voltage level as V_{SS}) for internal connection of input and I/O pins. No need to connect to external ground.
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
V_P	P	This pin is the segment pre-charge voltage reference pin. A capacitor should be connected between this pin and V_{SS} to enhance pre-charge voltage stability if necessary. When external capacitor is not used, this pin should be kept NC. No external power supply is allowed to connect to this pin.
VBREF	O	This is a reserved pin. It should be kept NC.
I_{REF}	I	This pin is the segment output current reference pin. I_{REF} is supplied externally. A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. Please refer to Figure 6-15 for the details of resistor value. When internal I_{REF} is used, this pin should be kept NC.

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>BS[2:0]</td><td>I</td><td>MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select.

Table 5-2 : Bus Interface selection

<table>
<tr><td>BS[2:0]</td><td>Interface</td></tr>
<tr><td>000</td><td>4 line SPI</td></tr>
<tr><td>001</td><td>3 line SPI</td></tr>
<tr><td>010</td><td>I^2C</td></tr>
<tr><td>110</td><td>8-bit 8080 parallel</td></tr>
<tr><td>100</td><td>8-bit 6800 parallel</td></tr>
</table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}</td></tr>
<tr><td>CL</td><td>I</td><td>This is external clock input pin.

When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.</td></tr>
<tr><td>CLS</td><td>I</td><td>This is internal clock enable pin.

When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.</td></tr>
<tr><td>CS#</td><td>I</td><td>This pin is the chip select input connecting to the MCU.
The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).</td></tr>
<tr><td>RES#</td><td>I</td><td>This pin is reset signal input.

When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>D/C#</td><td>I</td><td>This pin is Data/Command control pin connecting to the MCU.

When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.
When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.
In I^2C mode, this pin acts as SA0 for slave address selection.
When 3-wire serial interface is selected, this pin must be connected to V_{SS}.

For detail relationship to MCU interface signals, refer to Timing Characteristics Diagrams at Figure 8-3</td></tr>
<tr><td>R/W# (WR#)</td><td>I</td><td>This pin is read / write control input pin connecting to the MCU interface.

When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.

When serial or I^2C interface is selected, this pin must be connected to V_{SS}.</td></tr>
</table>

Pin Name	Pin Type	Description
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D2, D1 should be tied together as the serial data input: SDIN, and D0 will be the serial clock input: SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.
T0	I/O	This is a reserved pin. It should be kept NC.
T1	I/O	This is a reserved pin. It should be kept NC.
SEG0 ~ SEG159	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM0 ~ COM159	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
TR[15:0]	-	Reserved pin and is recommended to keep it float.
NC	-	This is dummy pin. It should be kept NC.

6 FUNCTIONAL BLOCK DESCRIPTIONS

6.1 MCU Interface selection

SSD1320 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 5-2 for BS[2:0] setting).

Table 6-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					SDIN		SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					SDIN		SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 and D2 should be tied together as the serial data input: SDIN.

6.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

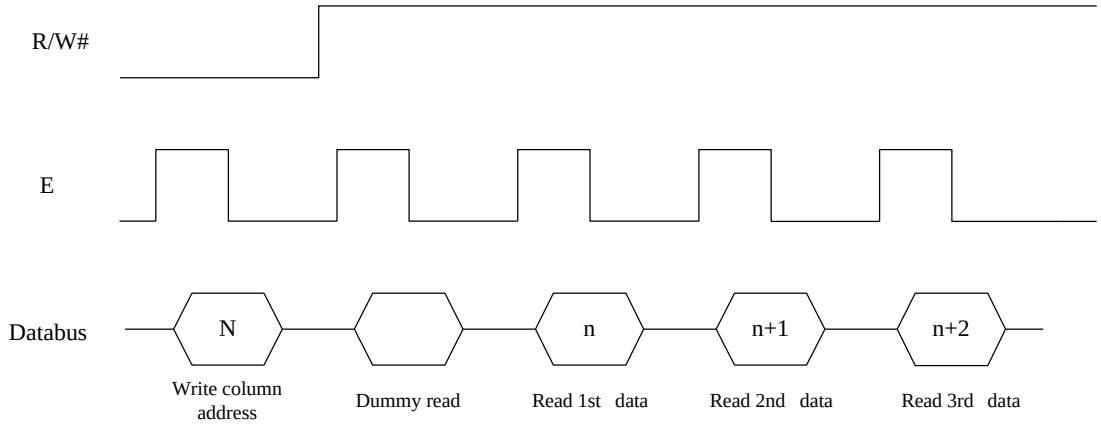
Table 6-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-1.

Figure 6-1 : Data read back procedure - insertion of dummy read



6.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 6-2 : Example of Write procedure in 8080 parallel interface mode

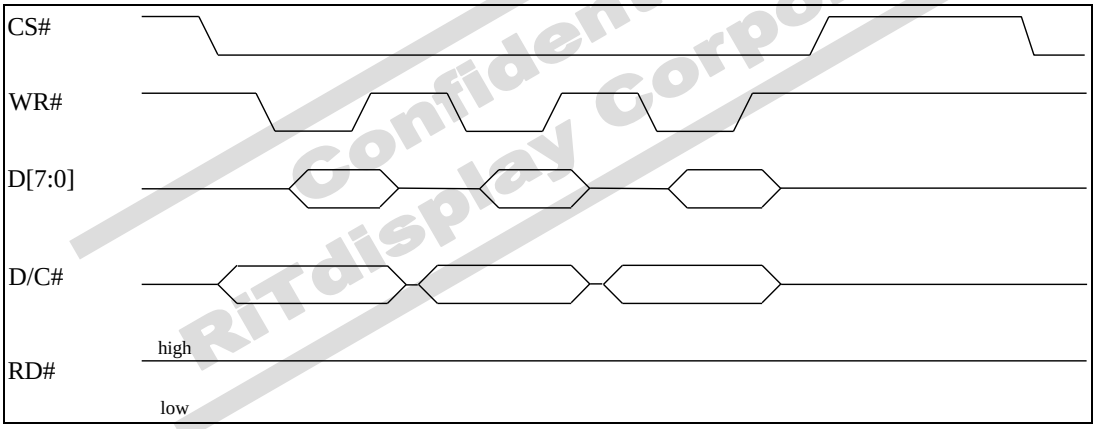


Figure 6-3 : Example of Read procedure in 8080 parallel interface mode

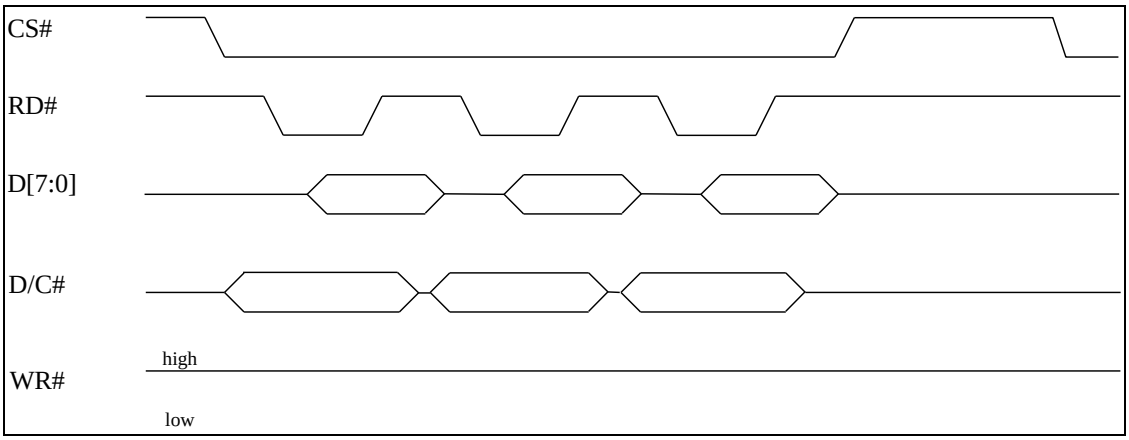


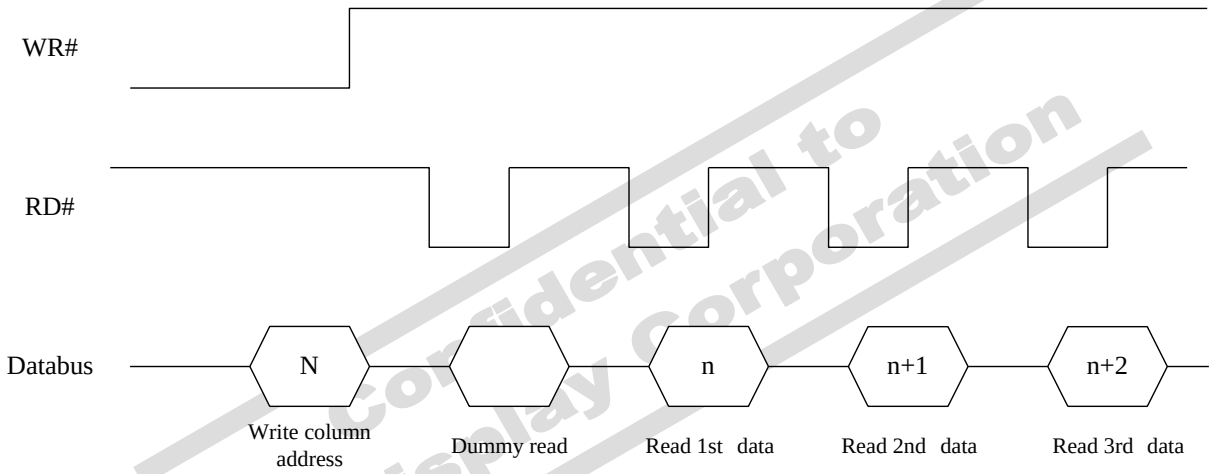
Table 6-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-4.

Figure 6-4 : Display data read back procedure - insertion of dummy read



6.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 and D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, E(RD#) and R/W#(WR#) can be connected to an external ground.

Table 6-4 : Control pins of 4-wire Serial interface

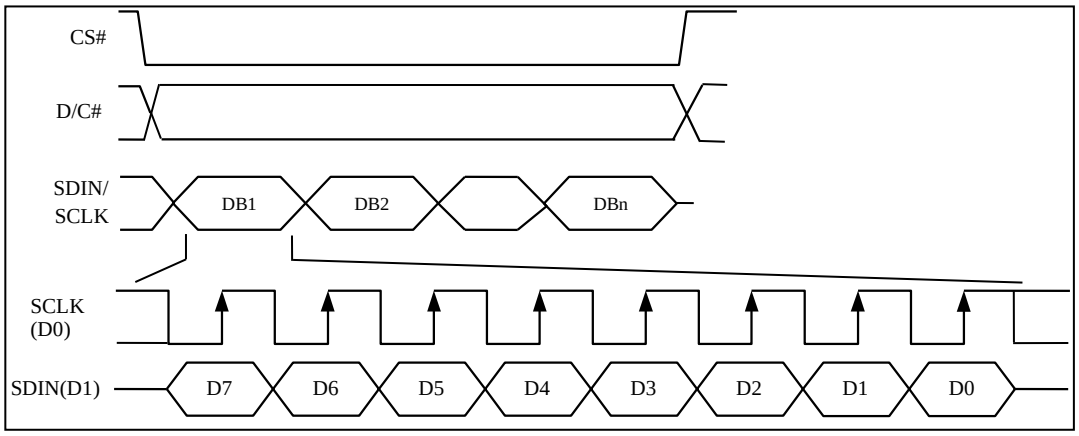
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ..., D0. D/C# is sampled on every eighth clock and D/C# should be kept stable throughout eight clock period. The data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 6-5 : Write procedure in 4-wire Serial interface mode



6.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 and D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

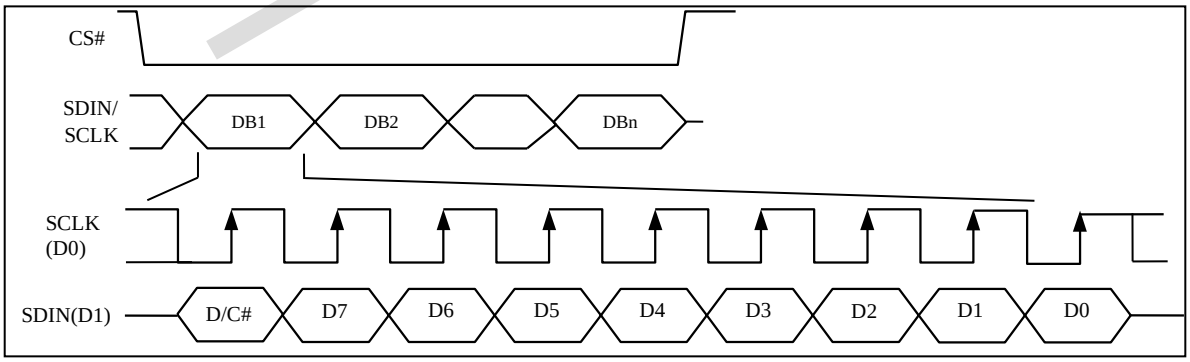
Under serial mode, only write operations are allowed.

Table 6-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 6-6 : Write procedure in 3-wire Serial interface mode



6.1.5 MCU I^2C Interface

The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1320 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1320. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I^2C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

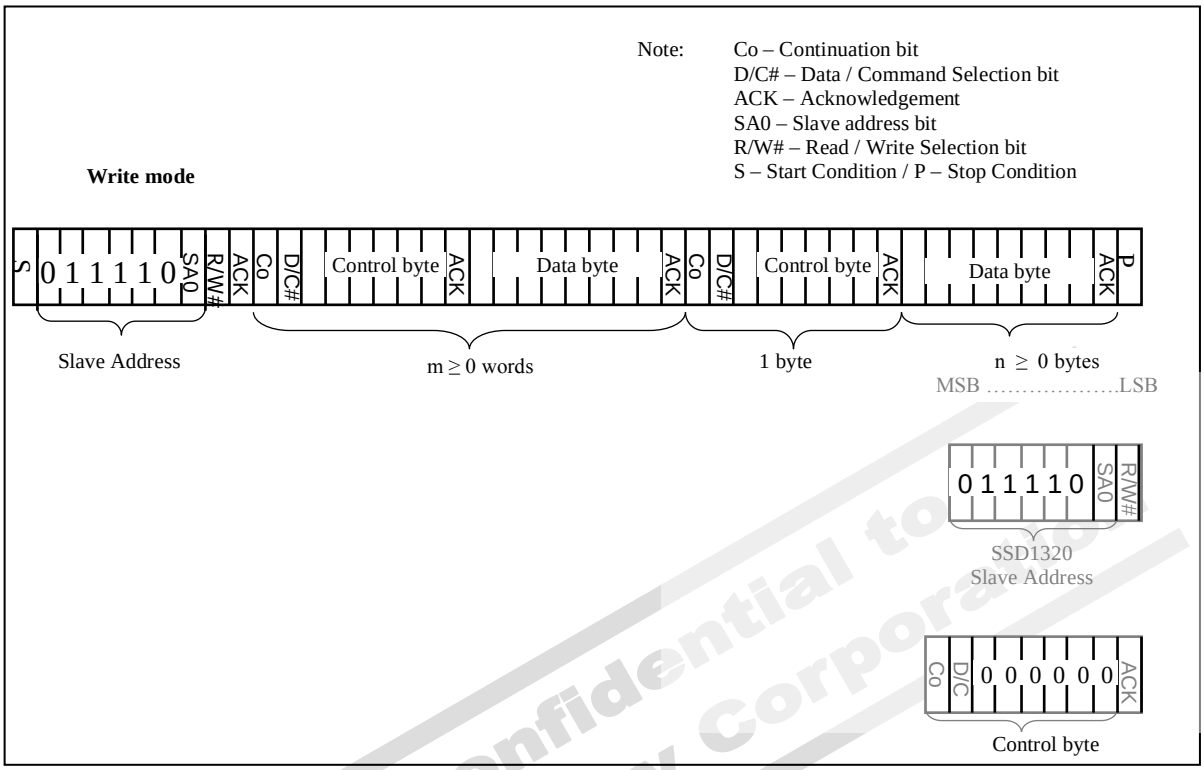
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.

c) I^2C-bus clock signal (SCL)
The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

6.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 6-7 for the write mode of I²C-bus in chronological order.

Figure 6-7 : I²C-bus data format



6.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1320, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 6-9 : Definition of the acknowledgement condition for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 6-8 : Definition of the Start and Stop Condition

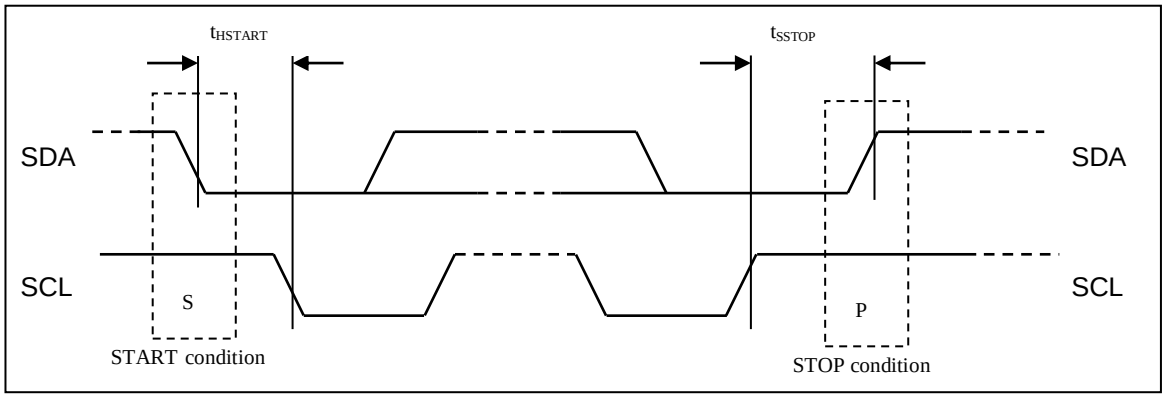
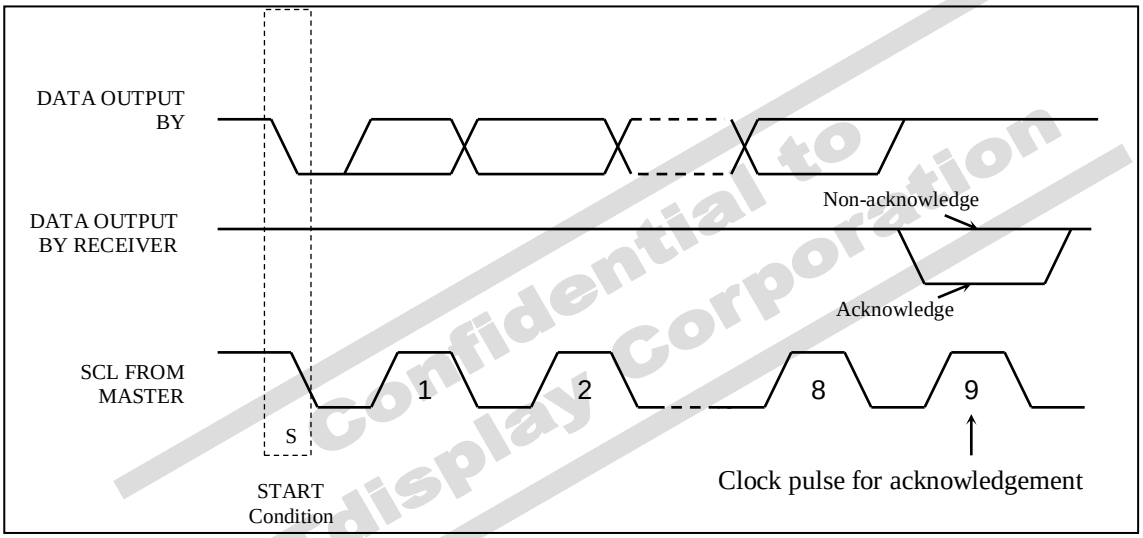


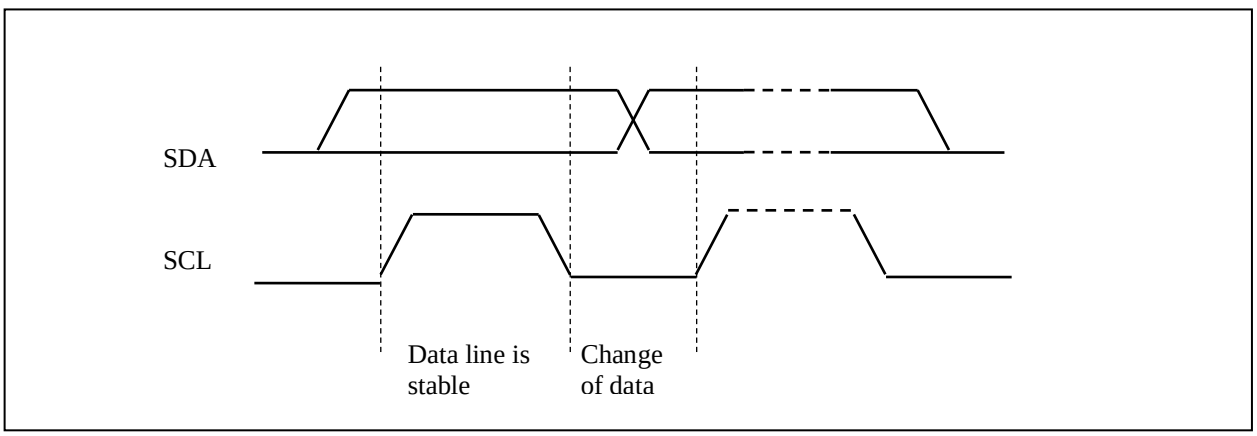
Figure 6-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 6-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 6-10 : Definition of the data transfer condition



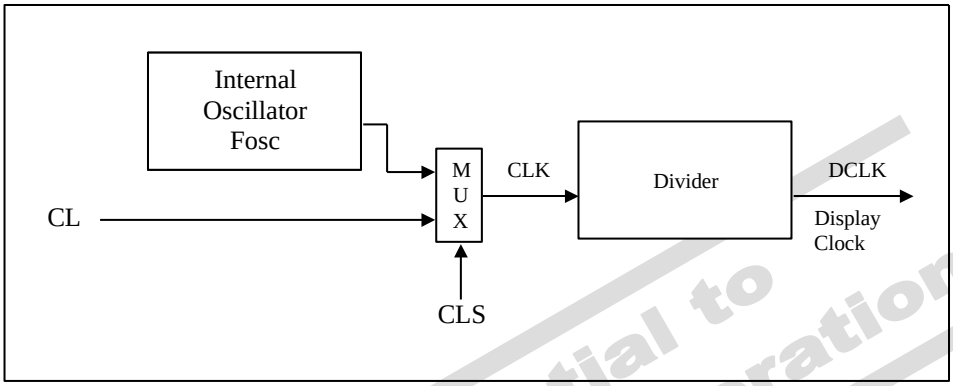
6.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

6.3 Oscillator Circuit and Display Time Generator

Figure 6-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 256 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

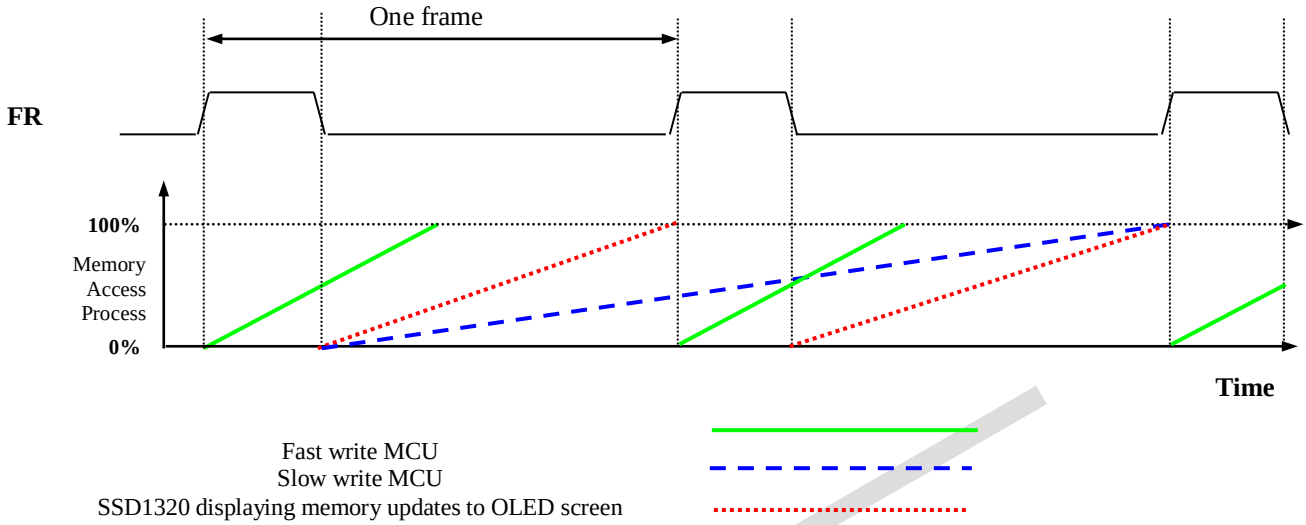
$$F_{FRM} = \frac{F_{osc}}{D \times K \times No.\,of\ Mux}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 256.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  = 7 + 2 + 66 = 75 at power on reset (that is K_0 is a constant that equals to 66)
  Please refer to Section 6.6 for the details of the "Phase".
- Number of multiplex ratio is set by command A8h. The power on reset value is 159 (i.e. 160MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

6.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

6.5 Reset Circuit

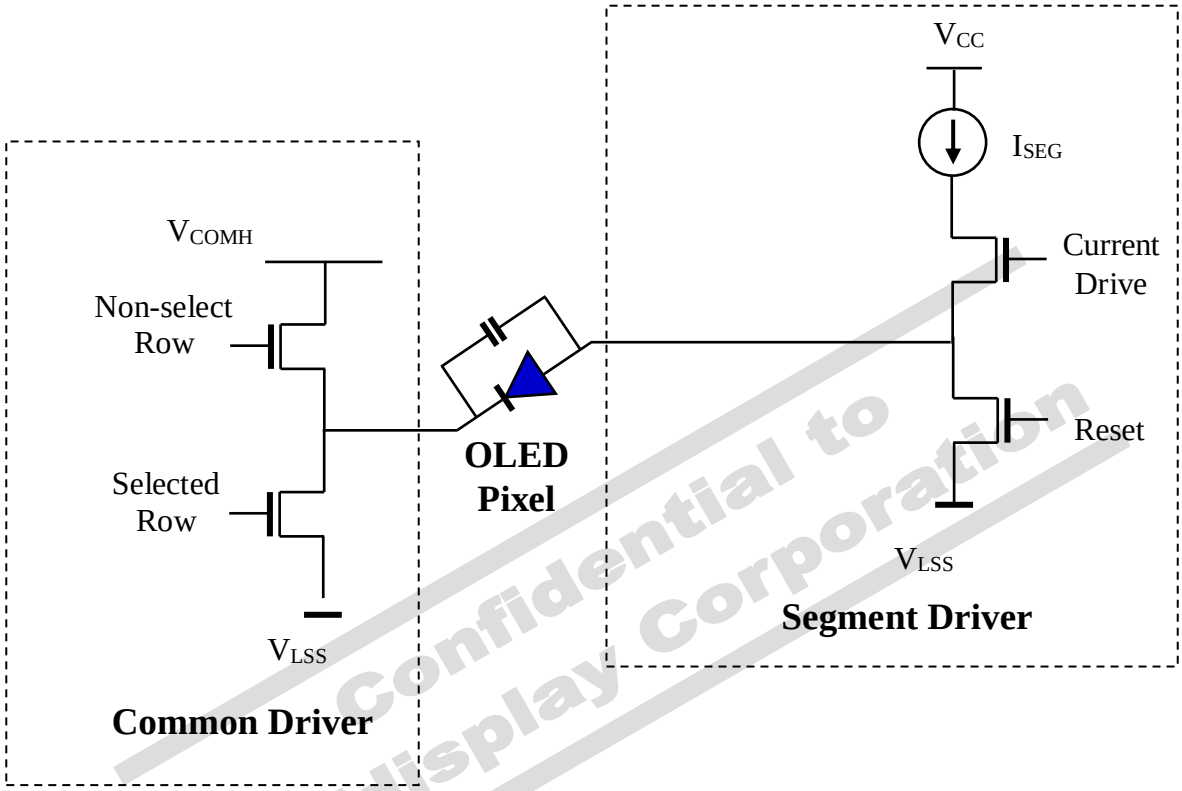
When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 160 x 160 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

6.6 Segment Drivers/Common Drivers

Segment drivers have 160 current sources to drive OLED panel. The driving current can be adjusted up to 600uA with 8 bits, 256 steps by contrast setting command (81h). Common drivers generate voltage scanning pulses. The block diagrams and waveforms of the segment and common driver are shown as follow.

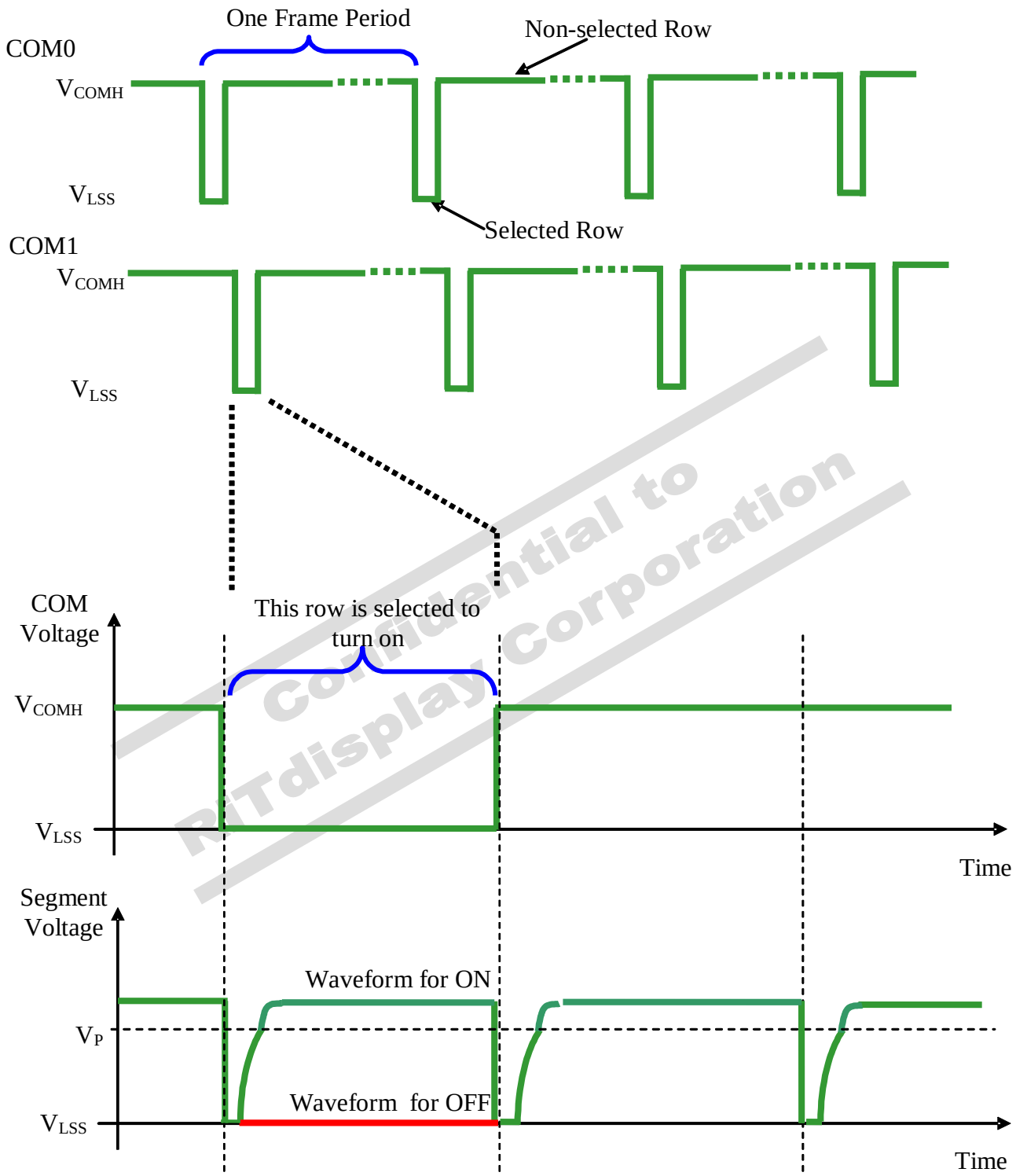
Figure 6-12: Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 6-13.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins.

Figure 6-13 : Segment and Common Driver Signal Waveform



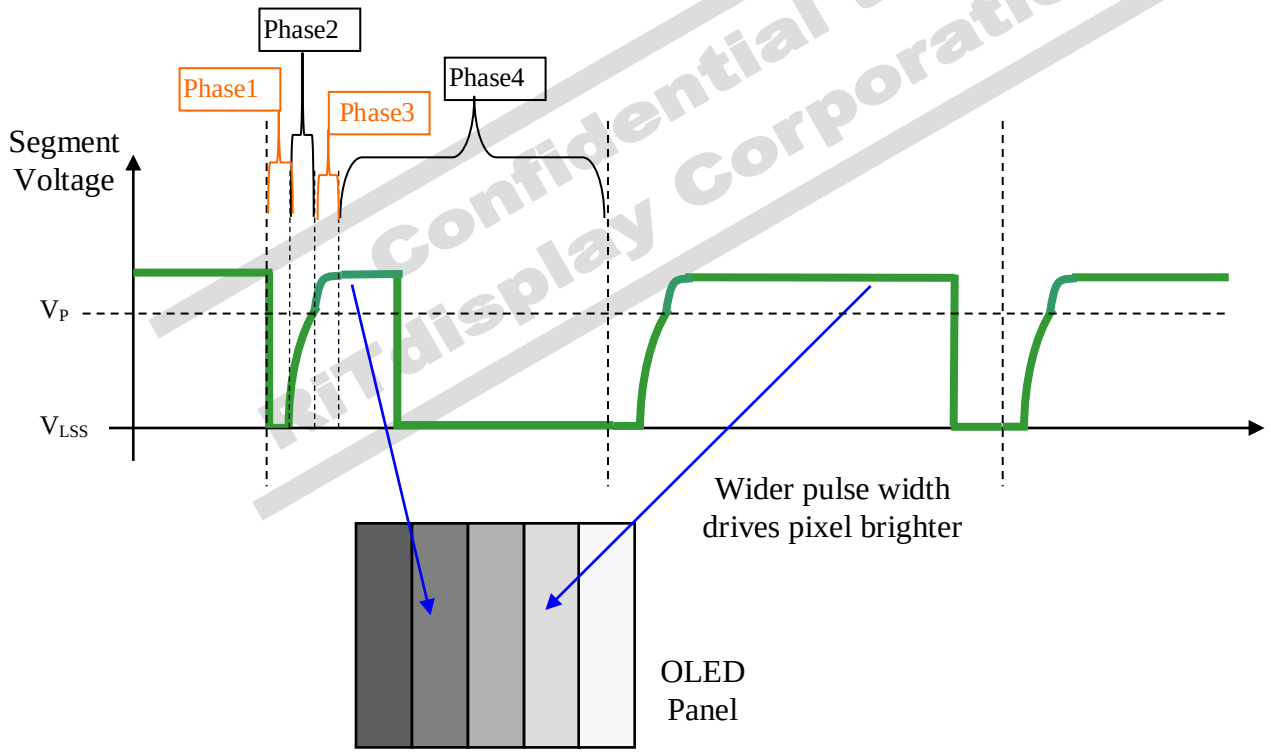
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command D9h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS}. The amplitude of V_P can be programmed by the command BCh. The period of phase 2 can be programmed by command D9h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command DCh.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command BEh/BFh. The bigger gamma setting (the wider pulse widths) in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

Figure 6-14 : Gray Scale Control by PWM in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command BEh/BFh. In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

6.7 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 160x160x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps in Table 6-6 to Table 6-10 show some examples to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D12797, D12798, D12799 represent the 160x160 data bytes in the GDDRAM.

These are the commands for Re-map setting:

Description	Type	Register
Disable/Enable Column Address Re-map	Single Byte	A0h/A1h
Horizontal/Vertical Address Increment	Double Byte	20h 00h/01h
Disable/Enable COM Re-map	Single Byte	C0h/C8h
Disable/Enable Portrait Mode	Double Byte	25h 00h/01h

Table 6-6 shows the GDDRAM map under the following condition:

- Command Setting:

Disable Column Address Re-map	A0h
Horizontal Address Increment	20h 00h
Disable COM Re-map	C0h
Disable Portrait Mode	25h 00h

- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D12799

Table 6-6 : GDDRAM address map 1

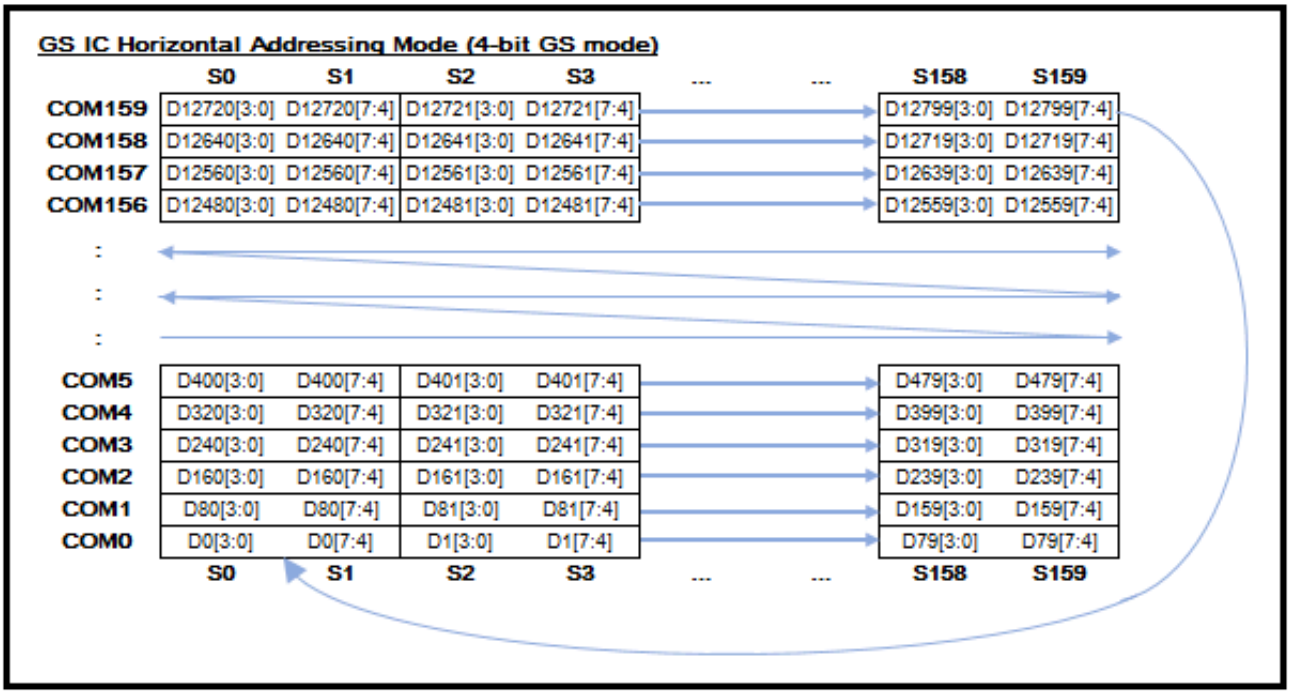


Table 6-7 shows the GDDRAM map under the following condition:

- Command Setting:

Disable Column Address Re-map	A0h
Vertical Address Increment	20h 01h
Disable COM Re-map	C0h
Disable Portrait Mode	25h 00h

- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D12799

Table 6-7 : GDDRAM address map 2

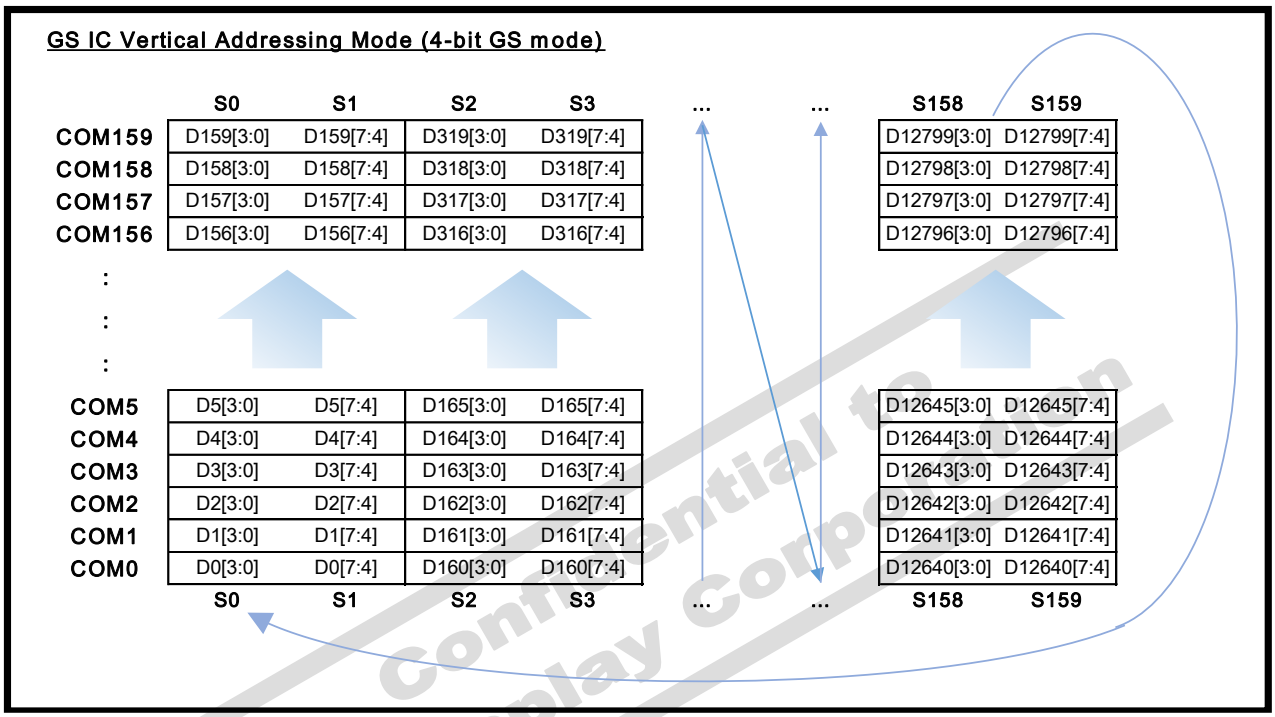


Table 6-8 shows the GDDRAM map under the following condition:

- Command Setting:

Enable Column Address Re-map	A1h
Horizontal Address Increment	20h 00h
Disable COM Re-map	C0h
Disable Portrait Mode	25h 00h

- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D12799

Table 6-8 : GDDRAM address map 3

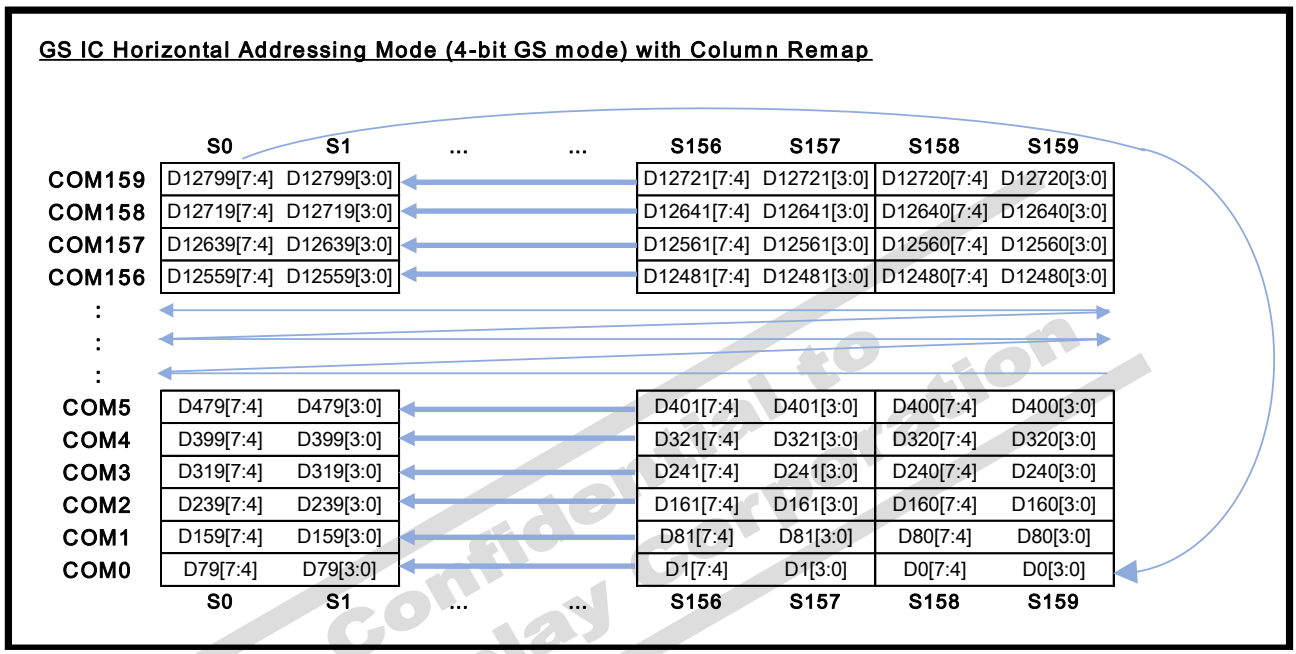


Table 6-9 shows the GDDRAM map under the following condition:

- Command Setting:

Disable Column Address Re-map	A0h
Horizontal Address Increment	20h 00h
Enable COM Re-map	C8h
Disable Portrait Mode	25h 00h

- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D12799

Table 6-9 : GDDRAM address map 4

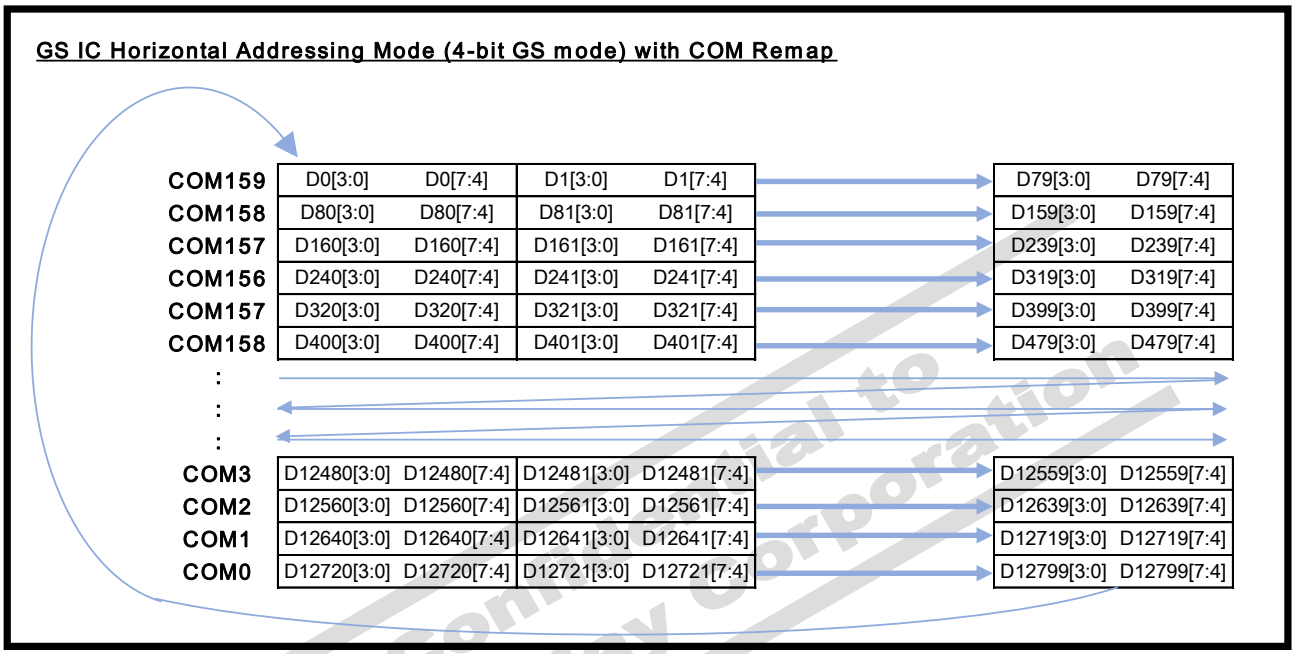


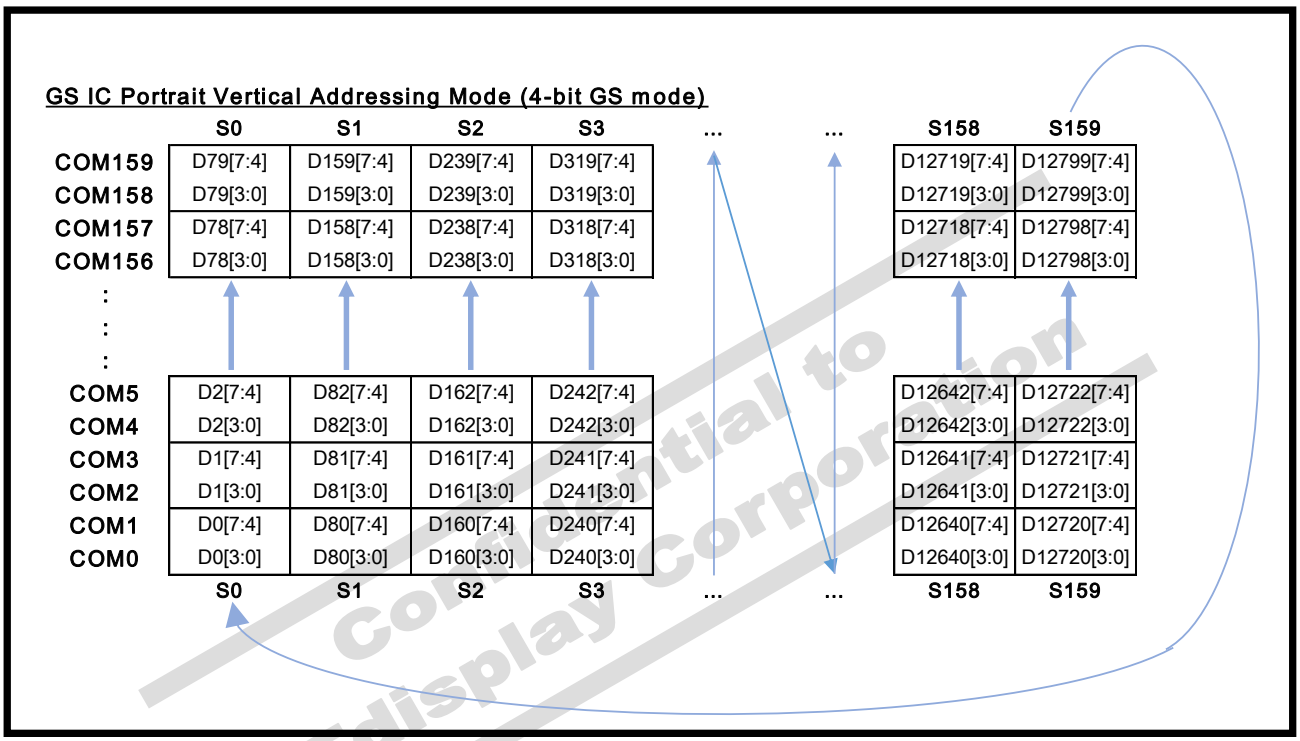
Table 6-10 shows the GDDRAM map under the following condition:

- Command Setting:

Disable Column Address Re-map	A0h
Vertical Address Increment	20h 01h
Disable COM Re-map	C0h
Enable Portrait Mode	25h 01h

- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D12799

Table 6-10 : GDDRAM address map 5



6.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

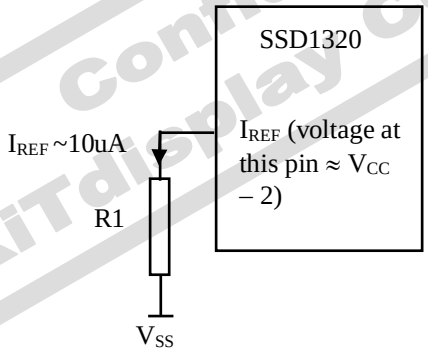
  I_{SEG} = Contrast / 4 x I_{REF}

  in which the contrast (1~255) is set by Set Contrast command 81h

  When internal I_{REF} is used, the I_{REF} pin should be kept NC.
  Bit A[4] of command ADh is used to select external or internal I_{REF} :
  A[4] = '0' Select external I_{REF} [Reset]
  A[4] = '1' Enable internal I_{REF} during display ON

When external I_{REF} is used, the magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 6-15 : I_{REF} Current Setting by Resistor Value. It is recommended to set I_{REF} to 10 ± 2uA so as to achieve I_{SEG} = 600uA at maximum contrast 255.

Figure 6-15 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 2V, the value of resistor R1 can be found as below:

For I_{REF} = 10uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 2) / 10uA
= 1MΩ

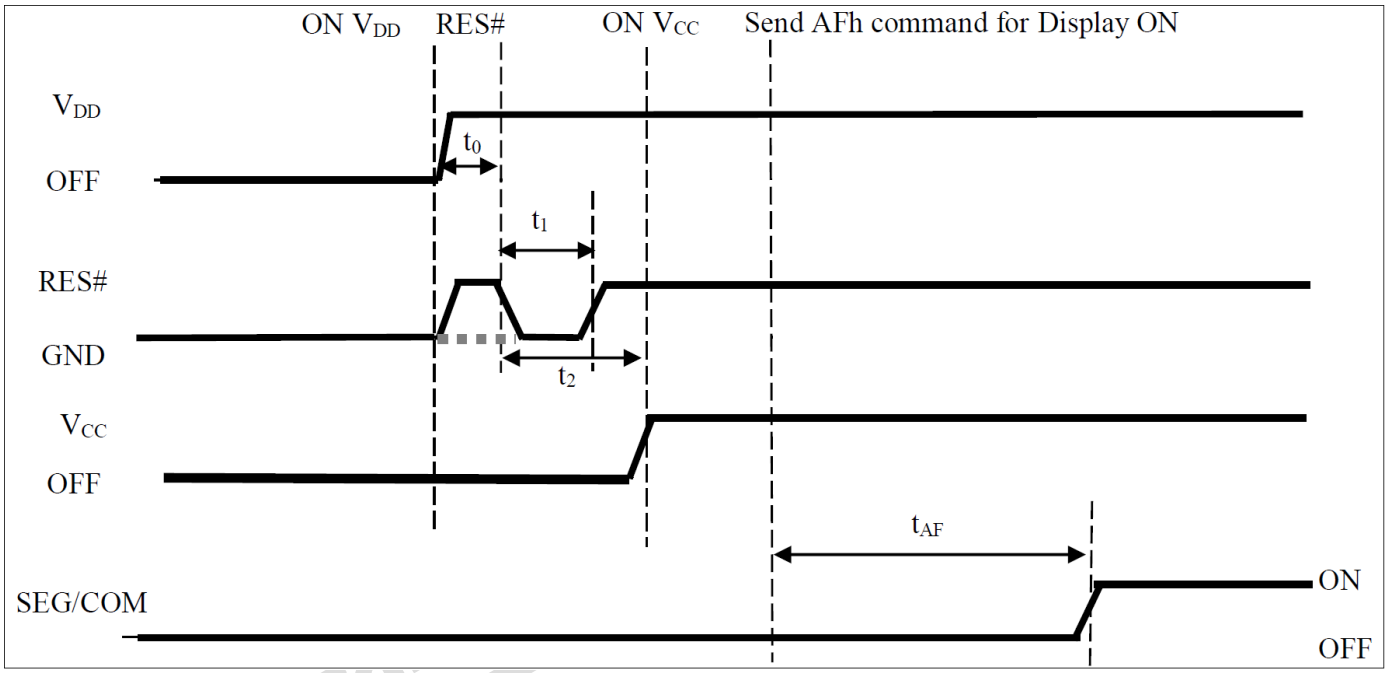
6.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1320.

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

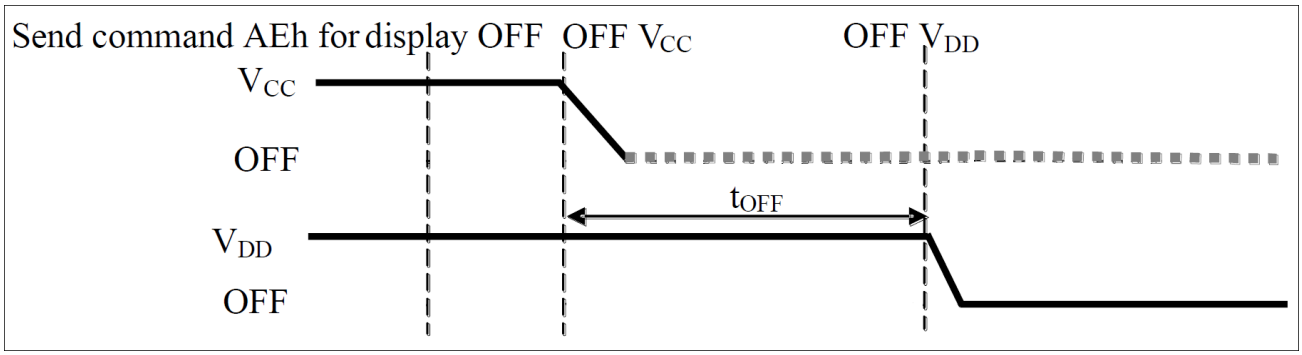
Figure 6-16 : Power ON Sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2]
3. Power OFF V_{DD} after t_{OFF}. [4] (where Minimum t_{OFF}=0ms, typical t_{OFF}=100ms)

Figure 6-17 : Power OFF Sequence



Note:

[1] V_{CC} should be kept float (i.e. disable) when it is OFF.
[2] Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
[3] The register values are reset after t_1.
[4] V_{DD} should not be Power OFF before V_{CC} Power OFF.

MAXIMUM RATINGS

Table 0-1 : Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 4.0	V
V_{CC}		-0.5 to 19.0	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	℃
T_{stg}	Storage Temperature Range	-65 to +150	℃

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

7 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 1.65V to 3.5V

T_A = 25°C

Table 7-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	8	-	18	V
V_{DD}	Logic Supply Voltage	-	1.65	2.8	3.5	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 10MHz	0.9 x V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 10MHz	0	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	-	0	-	0.2 x V_{DD}	V
$I_{DD,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.5V, V_{CC} = 8V~18V Display OFF, No panel attached	-	-	10	uA
$I_{CC,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.5, V_{CC} = 8V~18V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =15V, I_{REF} = 10uA, No loading, Display ON, All ON	Contrast = FFh	-	TBD	TBD	uA
I_{DD}	V_{DD} Supply Current V_{DD} =2.8V, V_{CC} = 15V, I_{REF} =10uA , No loading, Display ON, All ON	Contrast = FFh	-	TBD	TBD	uA
I_{SEG}	Segment Output Current, V_{DD} = 2.8V, V_{CC}=15V, I_{REF}=10uA, Display ON.	Contrast=FFh	-	600	-	uA
		Contrast=7Fh	-	TBD	-	
		Contrast=3Fh	-	TBD	-	
I_{SEG} Dev	Segment Output Current, V_{DD} = 2.8V, V_{CC}=15V, I_{REF}=10uA, Display ON. Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:159] = Segment current at contrast setting = FFh	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

8 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=1.65 to 3.5V
T_A = 25°C

Table 8-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 1.8V	TBD	TBD	TBD	kHz
F_{FRM}	Frame Frequency	160x160 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx160)(2)	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h is in default value.

(2) D: divide ratio (default value = 2)
K: number of display clocks per row period (default value = 75)
Please refer to (Set Display Clock Divide Ratio/Oscillator Frequency, D5h) for detailed description

Table 8-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 8-1: 6800-series MCU parallel interface characteristics

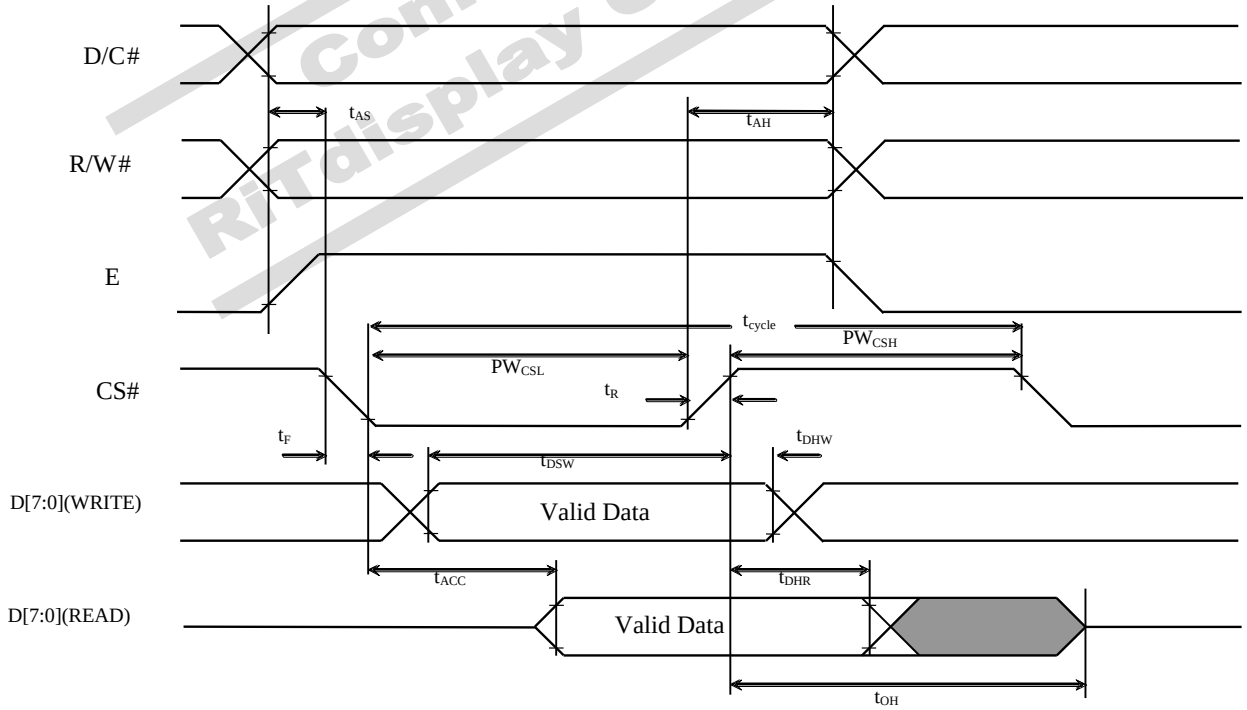
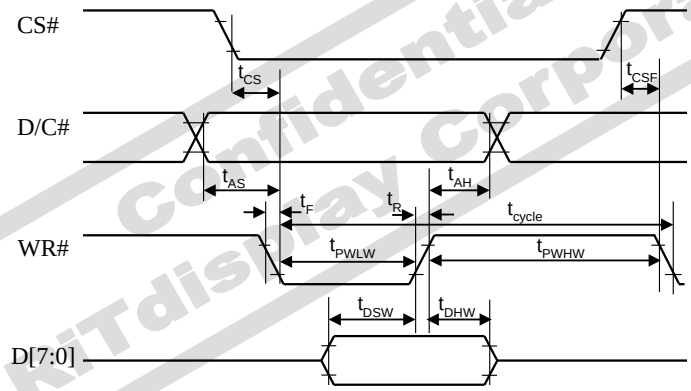


Table 8-3 : 8080-Series MCU Parallel Interface Timing Characteristics

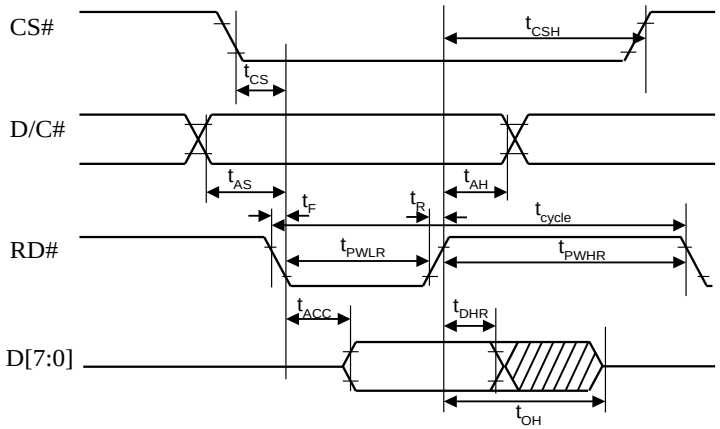
(V_{DD} - V_{SS} = 1.65V ~3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 8-2 : 8080-series parallel interface characteristics



Write cycle



Read Cycle

Table 8-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	66	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 8-3 : Serial interface characteristics (4-wire SPI)

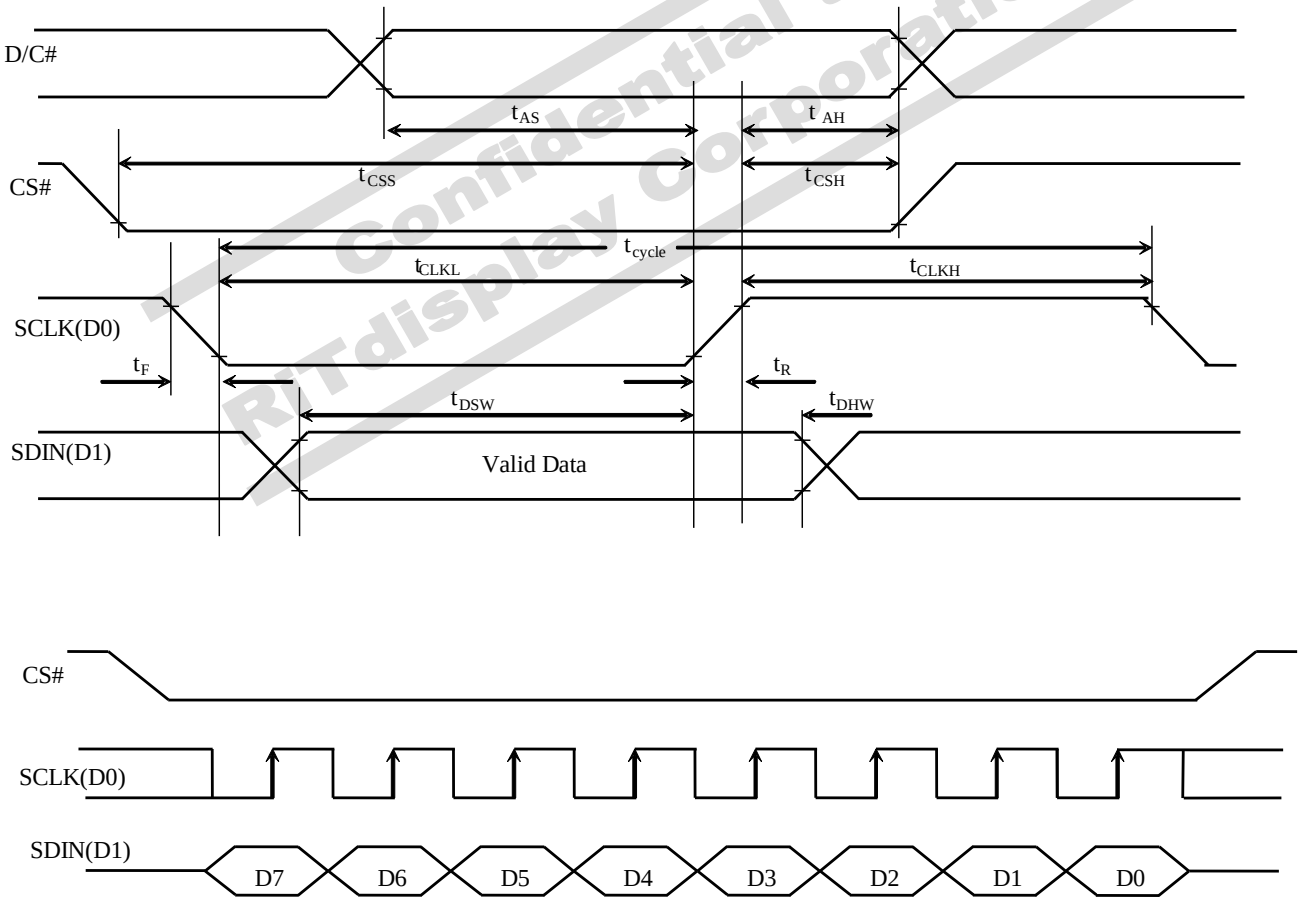


Table 8-5 : Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	66	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 8-4 : Serial interface characteristics (3-wire SPI)

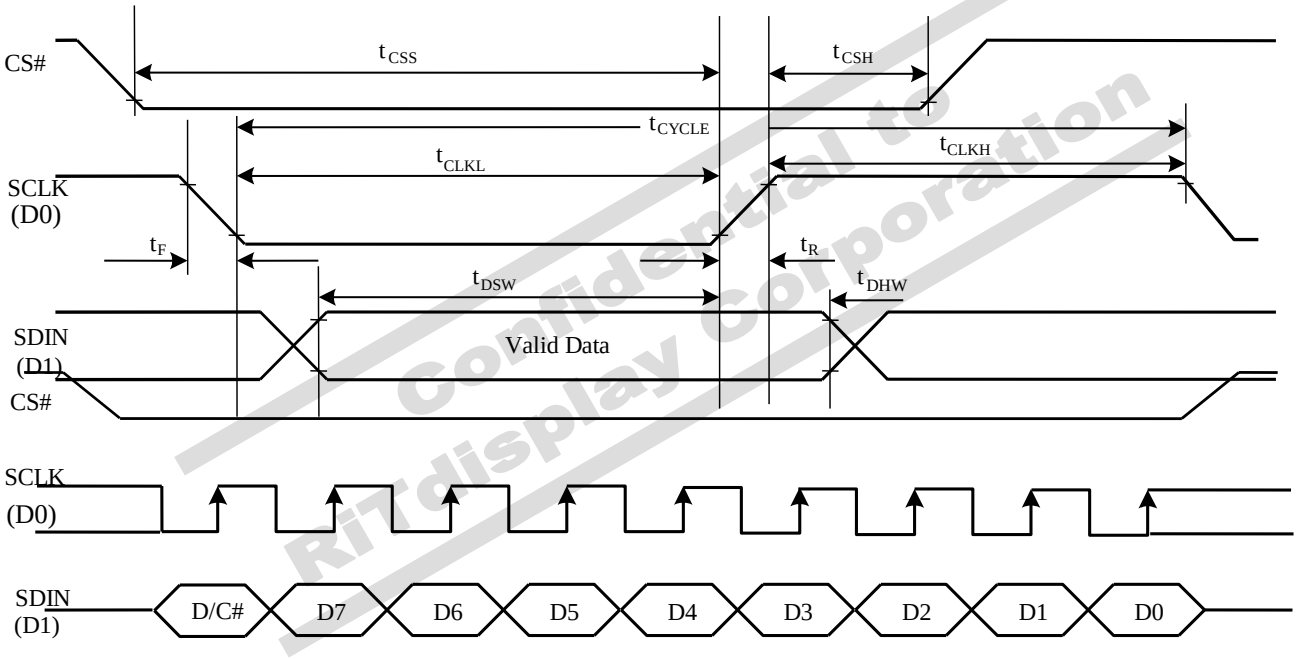
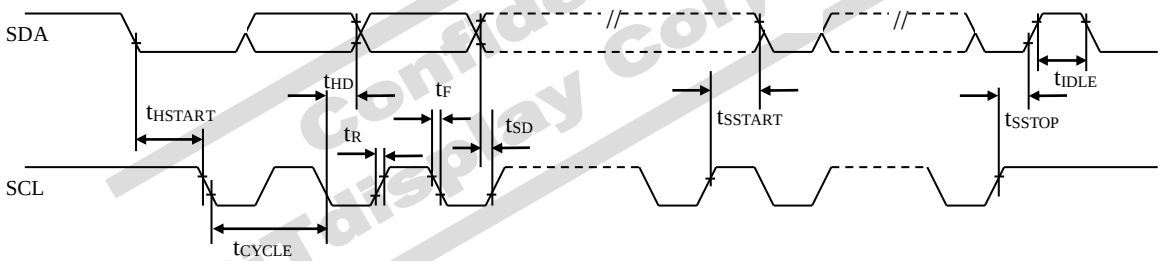


Table 8-6 : I²C Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V~3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

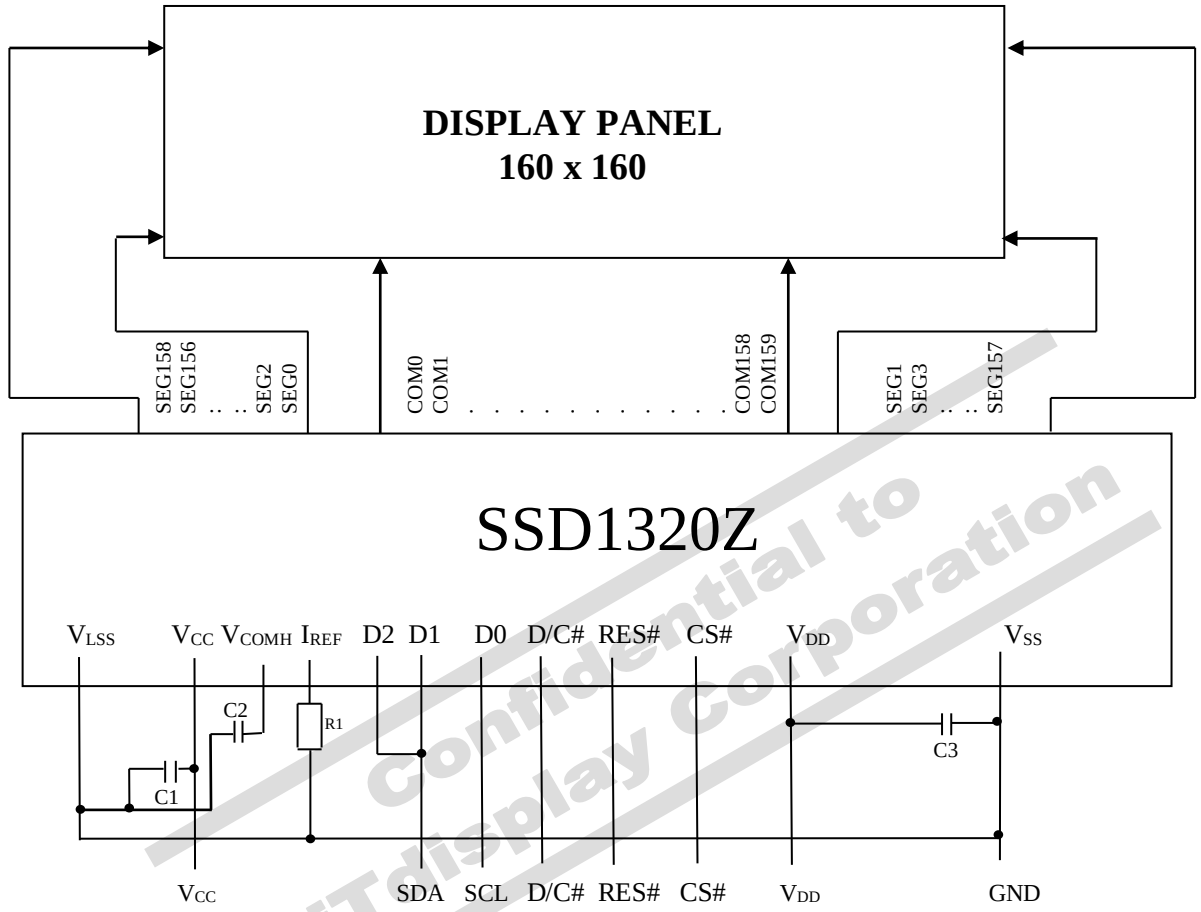
Figure 8-5 : I²C interface Timing characteristics



9 APPLICATION EXAMPLE

Figure 9-1 : Application Example of SSD1320Z

The configuration for 4-wire SPI interface mode is shown in the following diagram:
(V_{DD}=1.8V, V_{CC} =15V, I_{REF}=10uA)



Pin connected to MCU interface: D[2:0], RES#, D/C#, CS#
Pin internally connected to V_{LSS}: VSL
Pin internally connected to V_{SS} (or V_{LL}): D[7:3], BS[2:0], E, R/W#, CL, BGGND
Pin internally connected to V_{DD} (or V_{LL}): CLS
V_{BREF}, V_P, FR, T0, T1, TR[15:0], should be left open.

C1, C2: 2.2uF (1)
C3: 1.0uF (1) place close to IC V_{DD} and V_{SS} pins on PCB

Voltage at I_{REF} = V_{CC} – 2V. For V_{CC} = 15V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
≈ (15-2)V / 10uA
≈ 1.3MΩ

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face down.
(3) All V_{LSS} pads of the IC are recommended to be connected together to form a larger area of GND.
(4) V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard SJ/T 11363-2006 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)". Hazardous Substances test report is available upon request.

http://www.solomon-systech.com

APPENDIX SUMMARY

Reference	Item
APPENDIX I	SSD1320 Command Descriptions
APPENDIX II	SSD1320 Command Table

Appendix I: SSD1320 Command Descriptions

1 COMMAND DESCRIPTIONS

1.1 Fundamental Command

1.1.1 Set Memory Addressing Mode (20h)

There are 2 different memory addressing mode in SSD1320: horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above two modes.

1.1.2 Set Column Address (21h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

1.1.3 Set Row Address (22h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

1.1.4 Set Portrait Addressing Mode (25h)

This double byte command sets the way of memory addressing into portrait addressing mode or the normal (original) addressing mode. Horizontal or vertical addressing mode can be set on top of it by command 20h.

1.1.5 Set Contrast Control (81h)

This double byte command sets the Contrast Setting of the display, with a valid range from 01h to FFh. The segment output current increases as the contrast step value increases, which results in brighter display.

1.1.6 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design.

This command only affects subsequent data input. Data already stored in GDDRAM will have no change.

1.1.7 Set Display Start Line (A2h)

This double byte command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 159. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on.

1.1.8 Set Display Mode (A4h/A5h/A6h/A7h)

These are single byte commands and are used to set display status to Normal Display, Entire Display ON, Entire Display OFF or Inverse Display, respectively.

- Normal Display (A4h)
  Reset the "Entire Display ON" effect and turn the data to ON at the corresponding gray level. Figure 1-1 shows an example of Normal Display.

Figure 1-1: Example of Normal Display

Memory Display

- Set Entire Display ON (A5h)
  Force the entire display to be at gray scale level GS15, regardless of the contents of the display data RAM, as shown on Figure 1-2.

Figure 1-2: Example of Entire Display ON

Memory Display

- Normal Display (A6h)
  Reset the "Inverse Display" effect and turn the data to ON at the corresponding gray level. Figure 1-3 shows an example of Normal Display.

Figure 1-3: Example of Normal Display

Memory Display

- Inverse Display (A7h)
  The gray scale level of display data are swapped such that "GS0" ↔ "GS15", "GS1" ↔ "GS14", etc. Figure 1-4 shows an example of inverse display.

Figure 1-4: Example of Inverse Display

Memory Display

1.1.9 Set Multiplex Ratio (A8h)

This command switches the default 160 multiplex mode to any multiplex ratio, ranging from 16 to 160. The output pads COM0~COM159 will be switched to the corresponding COM signal.

1.1.10 External or internal IREF Selection (ADh)

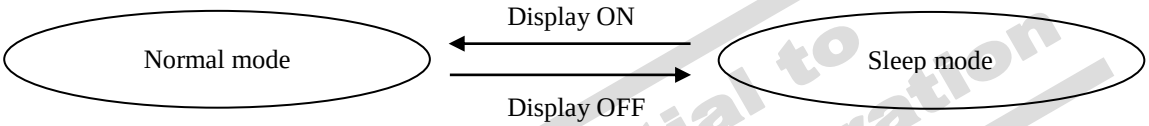
This double byte command supports External or Internal I_{REF} Selection.

1.1.11 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- Display OFF
- Display ON

Figure 1-5 : Transition between different modes



1.1.12 Set Pre-charge voltage (BCh)

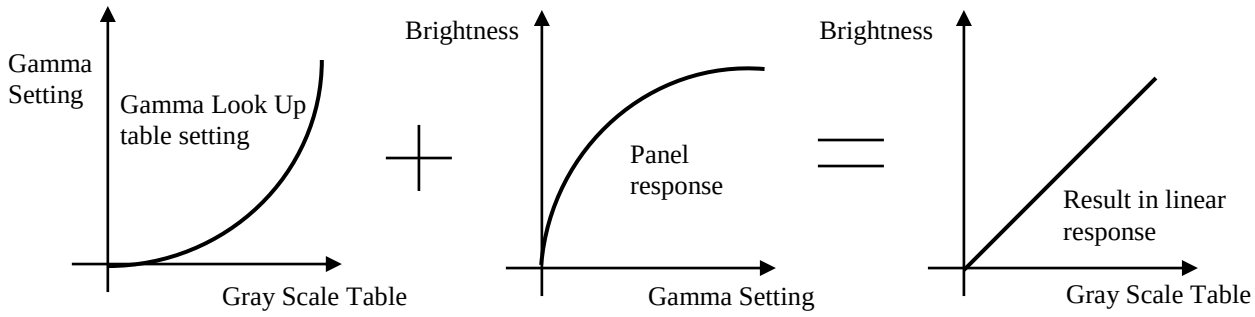
This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC}.

1.1.13 Set Gray Scale Table (BEh)

This command is used to set each individual gray scale level for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON. Following the command BEh, the user has to set the gray scale setting for GS1, GS2, …, GS14, GS15 one by one in sequence.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 1-6) can compensate this effect.

Figure 1-6 : Example of Gamma correction by Gamma Look Up table setting



1.1.14 Select Default Linear Gray Scale Table (BFh)

This single byte command reloads the preset linear Gray Scale table as GS0 =Gamma Setting 0, GS1 = Gamma Setting 4, GS2 = Gamma Setting 8, ..., GS14 = Gamma Setting 56, GS15 = Gamma Setting 60.

1.1.15 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately.

1.1.16 Set Display Offset (D3h)

This double byte command specifies the mapping of display start line to one of COM0~COM159 (assuming that COM0 is the display start line, display start line register equals to 0).

1.1.17 Set Display Clock Divide Ratio / Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D) (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 256, with reset value = 0001b.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings being available.

1.1.18 Set Phase Length (D9h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period for Phase 1 in the unit of DCLK. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.

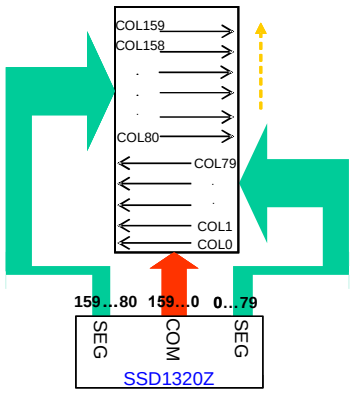
- Phase 2 (A[7:4]): Set the period for Phase 2 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P.

1.1.19 Set SEG Pins Hardware Configuration (DAh)

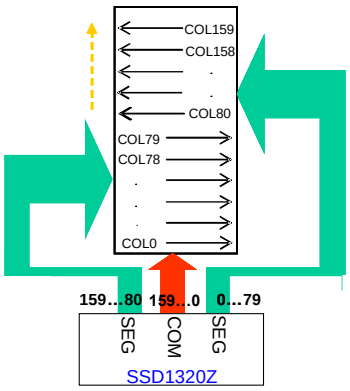
This command sets the SEG signals pin configuration to match the OLED panel hardware layout. SEG Odd / Even (Left / Right) and Top / Bottom connections are software selectable, thus there are total of 8 cases and they are shown on the followings:

Table 1-1: SEG Pins Hardware Configuration

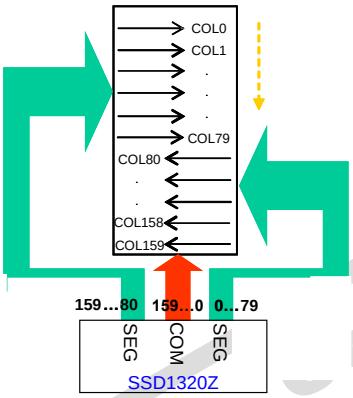
Case no.	Oddeven (1) / Sequential (0)	SEG Remap (0 disable, 1 enable)	Left / Right Swap	Remark
1	0	0	0	
2	0	0	1	
3	0	1	0	
4	0	1	1	
5	1	0	0	Default
6	1	0	1	
7	1	1	0	
8	1	1	1	



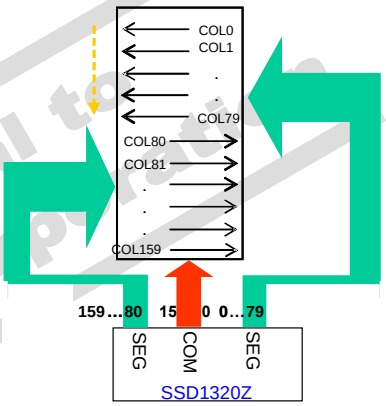
(1) Sequential SEG



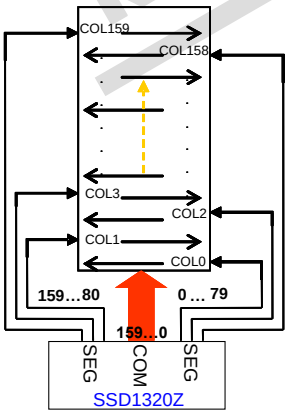
(2) Sequential SEG & left / right swap



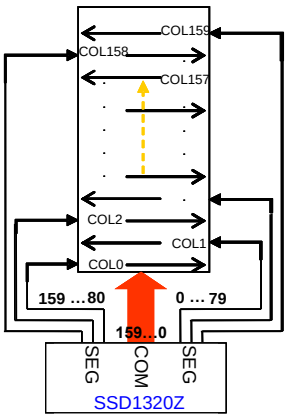
(3) Sequential SEG & SEG remap (with nibble remap)



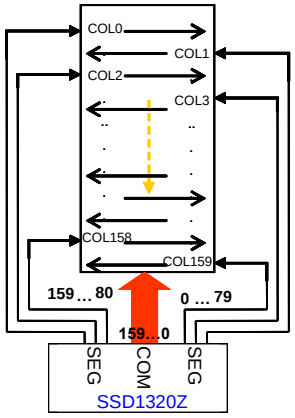
(4) Sequential SEG & SEG remap (with nibble remap) & left / right swap



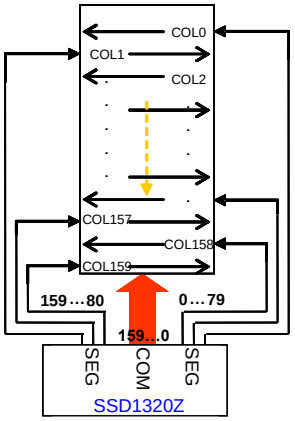
(5) Odd / even SEG



(6) Odd / even SEG & left / right swap



(7) Odd / even SEG & SEG remap (with nibble remap)



(8) Odd / even SEG & SEG remap (with nibble remap) & left / right swap

Note:

(1) The above eight figures are all with bump pads being faced up.

1.1.20 Set VCOMH Deselect Level (DBh)

This double byte command adjusts the VCOMH regulator output.

1.1.21 Set Command Lock (FDh)

This double byte command is used to lock the OLED driver IC from accepting any command except itself. After entering the "Lock" state, the OLED driver IC will not respond to any newly-entered command (except the register for unlocking it) and there will be no memory access. That means the OLED driver IC ignore all the commands (except the register for unlocking it) during the "Lock" state.

In the "Unlock" state, the driver IC resumes from the "Lock" state, and the driver IC will then respond to the command and memory access.

Appendix II: SSD1320 Command Table

1 COMMAND TABLE

Table 1-1: SSD1320 Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	20 A[0]	0 *	0 *	1 *	0 *	0 *	0 *	0 0	0 A_0	Set Memory Addressing Mode	A[0] = 0b, Horizontal Addressing Mode A[0] = 1b, Vertical Addressing Mode
0 0 0	21 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-79d, (RESET=0d) B[7:0]: Column end address, range : 0-79d, (RESET =79d)
0 0 0	22 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Row Address	Setup page start and end address A[7:0] : Row start address, range : 0-159d, (RESET=0d) B[7:0]: Row end address, range : 0-159d, (RESET =159d)
0 0	25 A[0]	0 *	0 *	1 *	0 *	0 *	1 *	0 0	1 A_0	Set Portrait Addressing Mode	A[0] = 0b, Normal Addressing Mode A[0] = 1b, Portrait Addressing Mode
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 79 is mapped to SEG0
0 0	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Start Line	Set display RAM display start line register from 0-159 by A[7:0] (RESET=00h) **Note** (1) In command A2h, A[6:0] from 00h to 3Fh has the same effect as command 40h-7Fh.
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[7:0] : from 16MUX to 160MUX. RESET = 1001 1111b (i.e. 159d, 160MUX) A[7:0] from 0 to 14 are invalid entry
0 0	AD A[4]	1 0	0 0	1 0	0 A_4	1 0	1 0	0 0	1 0	External or internal I_{REF} Selection	Select external or internal I_{REF}: A[4] = '0' Select external I_{REF} (RESET) A[4] = '1' Enable internal I_{REF} during display ON
0	AE/AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode
0	BC A[4:0]	1 *	0 *	1 *	1 A_4	1 A_3	1 A_2	0 A_1	0 A_0	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 11110b] A[4:0] | Hex code | pre-charge voltage 00000 | 00h | 0.10 x V_{CC} : | : | : 11110 | 1Eh | 0.50 x V_{CC} [reset] 11111 | 1Fh | 0.5133 x V_{CC} **Note** (1)Pre-charge voltage level must be smaller than COM deselect voltage level
0 0 0 … … … 0 0	BE A1[6:0] A2[6:0] … … … A14[6:0] A15[6:0]	1 * * … … … * *	0 $A1_6$ $A2_6$ … … … $A14_6$ $A15_6$	1 $A1_5$ $A2_5$ … … … $A14_5$ $A15_5$	1 $A1_4$ $A2_4$ … … … $A14_4$ $A15_4$	1 $A1_3$ $A2_3$ … … … $A14_3$ $A15_3$	1 $A1_2$ $A2_2$ … … … $A14_2$ $A15_2$	1 $A1_1$ $A2_1$ … … … $A14_1$ $A15_1$	0 $A1_0$ $A2_0$ … … … $A14_0$ $A15_0$	Set Gray Scale Table	The next 15 data bytes set the gray scale pulse width in unit of DCLK's. A1[6:0], value for GS1 level Pulse width A2[6:0], value for GS2 level Pulse width … A14[6:0], value for GS14 level Pulse width A15[6:0], value for GS15 level Pulse width **Note** (1) The pulse width value of GS1, GS2, ... , GS15 should not be equal. i.e. 0<GS1<GS2 … <GS15 (2) GS15 level pulse width must be set larger than the period of phase 1 + phase 2

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BF	1	0	1	1	1	1	1	1	Linear LUT	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 4 GS2 level pulse width = 8; GS3 level pulse width = 12; : : GS14 level pulse width = 56; GS15 level pulse width = 60
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~159d (RESET=0d)
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0]: Define divide ratio (D) of display clock (DCLK) (i.e. 1, 2, 4, 8…256) (RESET is 0001b, i.e. divide ratio = 2) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (RESET is 0100b) Range: 0000b~1111b.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[3:0] : Phase 1 period of up to 15 DCLK Clock 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK Clock 0 is invalid entry (RESET=7h)
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set SEG Pins Hardware Configuration	A[4]=0b, Sequential SEG pin configuration A[4]=1b (RESET), Alternative (odd/even) SEG pin configuration A[5]=0b (RESET), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap
0 0	DB A[2:0]	1 0	0 0	1 0	1 0	1 0	0 A_2	1 A_1	1 A_0	Set V_{COMH}	Set COM deselect voltage level. **A[5:3] / Hex code / V_{COMH} deselect level** 000b / 00h / ~ 0.72 x V_{CC} 010b / 10h / ~ 0.76 x V_{CC} 100b / 20h / ~ 0.80 x V_{CC} (RESET) 110b / 30h / ~ 0.84 x V_{CC}

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	FD	1	1	1	1	1	1	0	1	Set Command	A[2]: MCU protection status.
0	A[2]	0	0	0	1	0	A_2	1	0	Lock	A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command