SVC2002B Series

(20T202DA2JA)

VFD MODULE USER MANUAL

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Reference Controller Datasheet

Character VFD Selection Guide

1. SCOPE

This specification applies to VFD module (Model No.: 20T202DA2JA) manufactured by Samsung SDI.

2. FEATURES

2.1 Simple connection to the host system data bus via three-wired synchronous serial interface (/STB, SCK, SIO).

2.2 Since a DC-DC/AC converter is used, only +5Vdc power source is required to operate the module.

2.3 High quality of display and luminance.

2.4 Compact and light-weight unit by using new VFD technology and flat packed one-chip controller.

2.5 Luminance adjustment available by software (4 levels).

2.6 8 user definable fonts available (CG-RAM font).

2.7 ASCII and Japanese characters (CG-ROM font).

3. GENERAL DESCRIPTIONS

3.1 This specification becomes effective after being approved by the purchaser.

3.2 When any conflict is found in the specification, appropriate action shall be taken upon agreement of both parties.

3.3 The expected necessary service parts should be arranged by the customer before the completion of production.

4. PRODUCT SPECIFICATIONS

4.1 Type

Table_1

Type	20T202DA2JA
Digit Format	5x7 Dot Matrix with Cursor

4.2 Outer Dimensions, Weight (See Fig-5 on Page 6/17 for details)

Table_2

Parameter		Specification	Unit
Outer Dimensions	Width	116.0 +/-1.0	mm
	Height	37.0 +/-1.0	mm
	Thickness	18.7 Max	mm
Weight		Typical 50	g

4.3 Specifications of the Display Panel

Table_3

Parameter	Symbol	Specification	Unit
Display Size	W x H	70.8 x 11.5	mm
Number of Digit	-	20 Digits x 2 Lines	-
Character Size (excluding cursor)	W x H	2.4 x 4.7	mm
Character Pitch	-	3.6(H) / 6.1(V)	mm
Dot Size	W x H	0.4 x 0.5	mm
Display Color	-	Blue-Green (peak 505 nm)	-

4.4 Environment Conditions

Table_4

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature	Topr	-20	+70	°C
Storage Temperature	Tstg	-40	+85	°C
Humidity (Operating)	Hopr	0	85	%
Humidity (Non-operating)	Hstg	0	90	%
Vibration (10 ~ 55 Hz)	-	-	4	G
Shock	-	-	40	G

4.5 Absolute Maximum Ratings

Table_5

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	-0.5	6.0	V_{DC}
Input Signal Voltage	V_{IS}	-0.5	Vcc+0.5	V_{DC}

4.6 Recommend Operating Conditions

Table_6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V_{DC}
Signal (Logic) Input Voltage	V_{IS}	0	-	V_{CC}	V_{DC}
Operating Temperature	T_{OPR}	-20	+25	+70	°C

4.7 DC Characteristics (Ta=+25 °C, Vcc=+5.0 V_{DC})

Table_7

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Current *)		I_{CC}	-	150	220	mA
Logic Input Voltage	"H" Level	V_{IH}	0.8xV_{CC}	-	-	V_{DC}
	"L" Level	V_{IL}	-	-	0.2xV_{CC}	V_{DC}
"H" level Input current	V_{IN}=V_{CC}	I_{IH}	20	-	500	uA
Luminance		L	100 (340)	200 (680)	-	ft-L (cd/m^2)

*) Icc shows the current when all dots are turned on. The surge current can be approx. 3 times the specified supply current at power on. However, the exact peak surge current amplitude and duration are dependent on the characteristics of the host power supply.

4.8 Timing Chart and AC Characteristics

4.8.1 RESET Timing

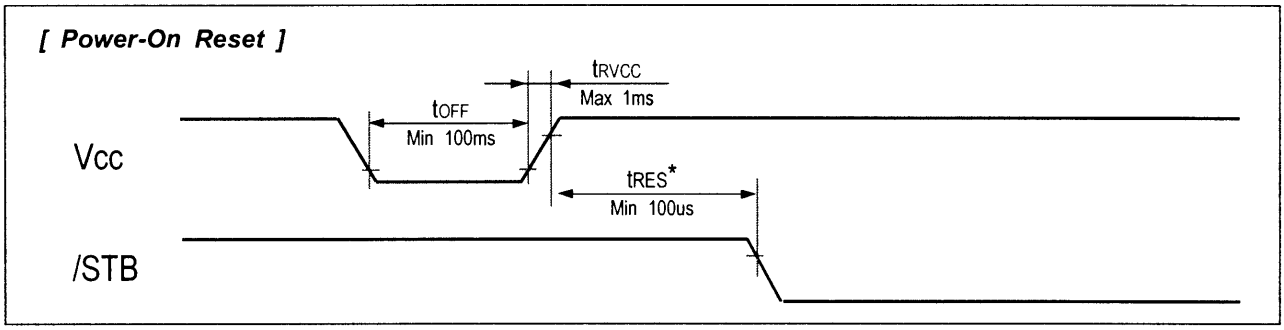


Fig-1. Power-on Reset and RESET signal Timing

4.8.2 Serial Input (Write) Timing

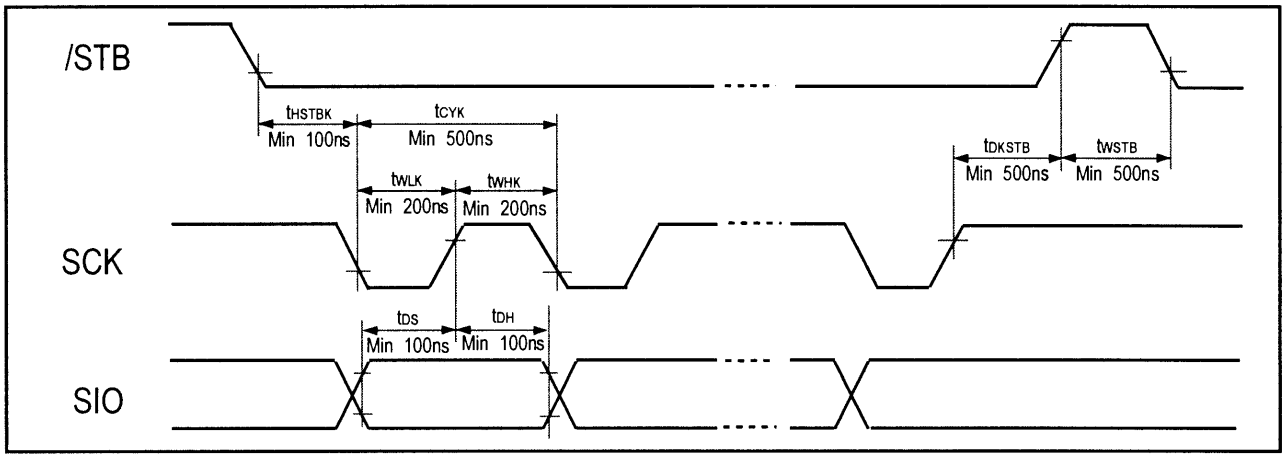


Fig-2. Data write-in Timing Diagram

4.8.3 Serial output (Read) Timing

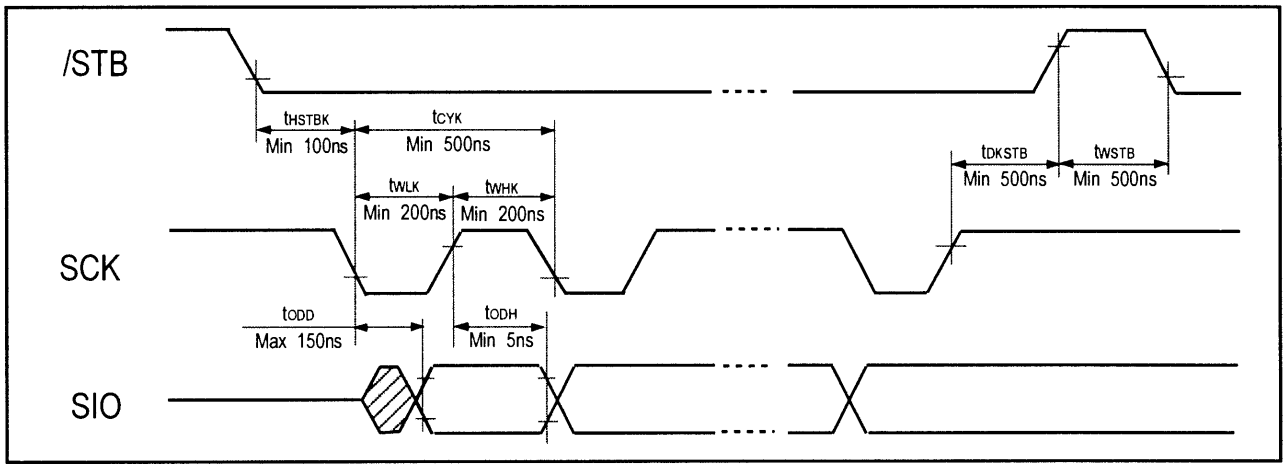


Fig-3. Data read-out Timing Diagram

4.9 Signal Interfacing

·Connector(Male) : 104426-3 (by AMP) or equivalent
See the Table_8 for description of each pin

Table 8

No.	Signal	Signal Description
1	GND	GND: Ground Terminal.
2	Vcc	Vcc : Power Supply Terminal. (+5Vdc is required.)
3	SIO	SIO : Input/Output Terminal for Display or Control Codes.
4	/STB	/STB: Strobe Input Terminal.
5	SCK	SCK: Shift Clock Input Terminal of Shift Register.

4.10 System Block Diagram

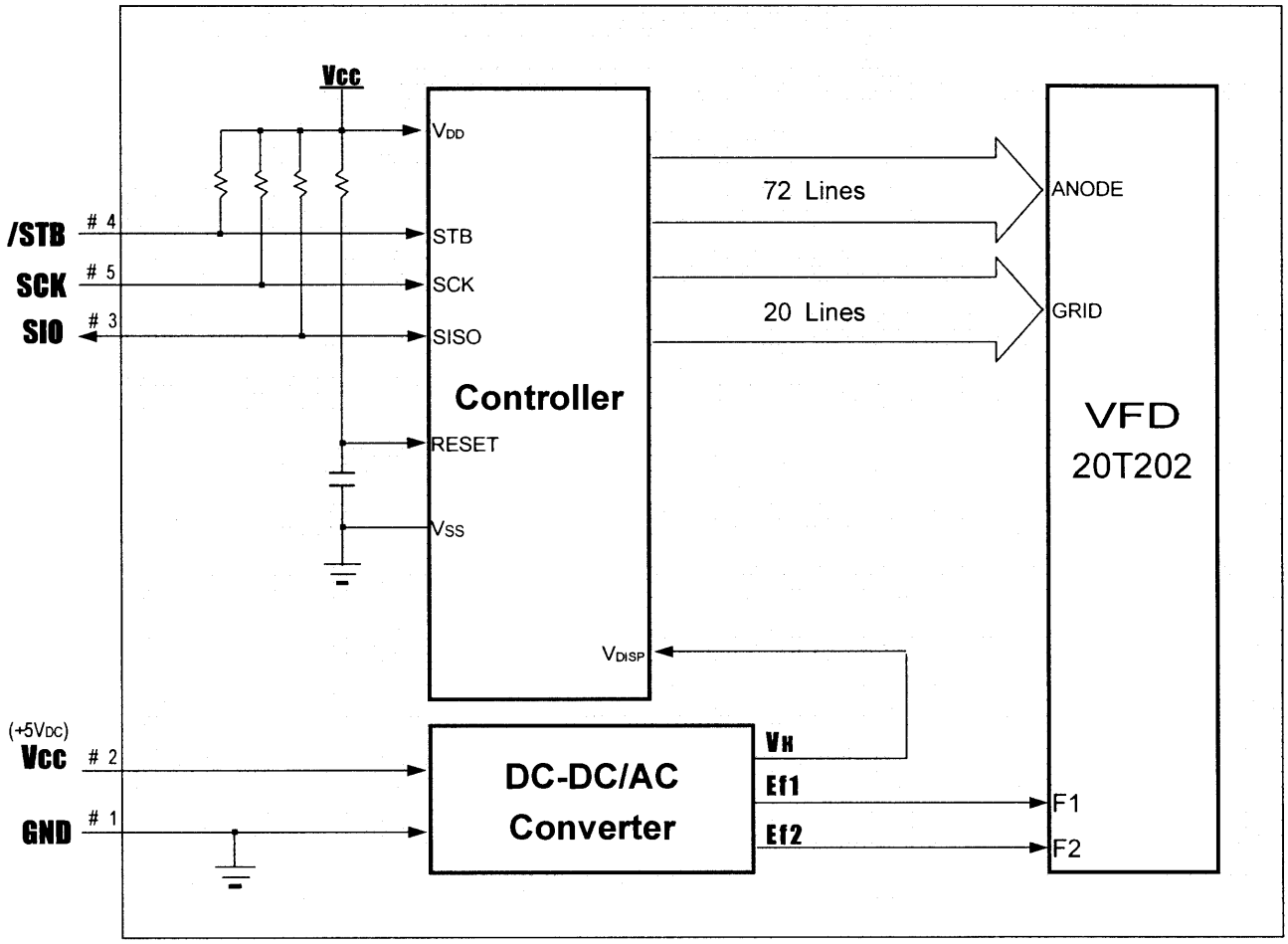


Fig-4. System Block Diagram of this VFD Module

4.11 Outer Dimensions

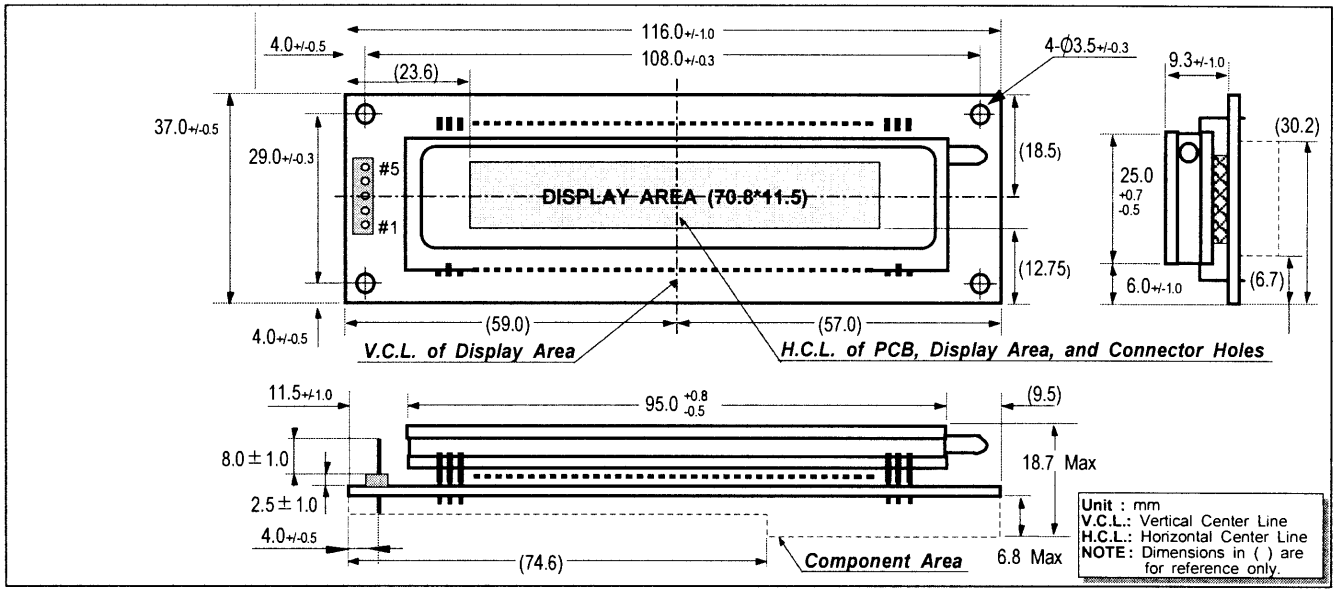


Fig-5. Outer Dimensions

4.12 Connector Cable Location

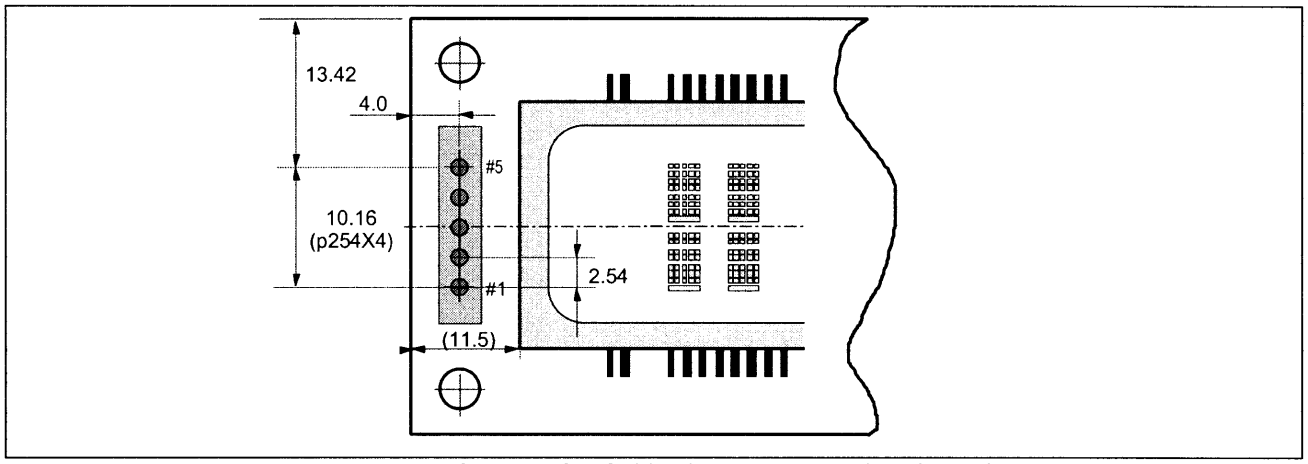


Fig-6. 5-pin Cable & Through hole Dimensions

4.13 Pattern Details

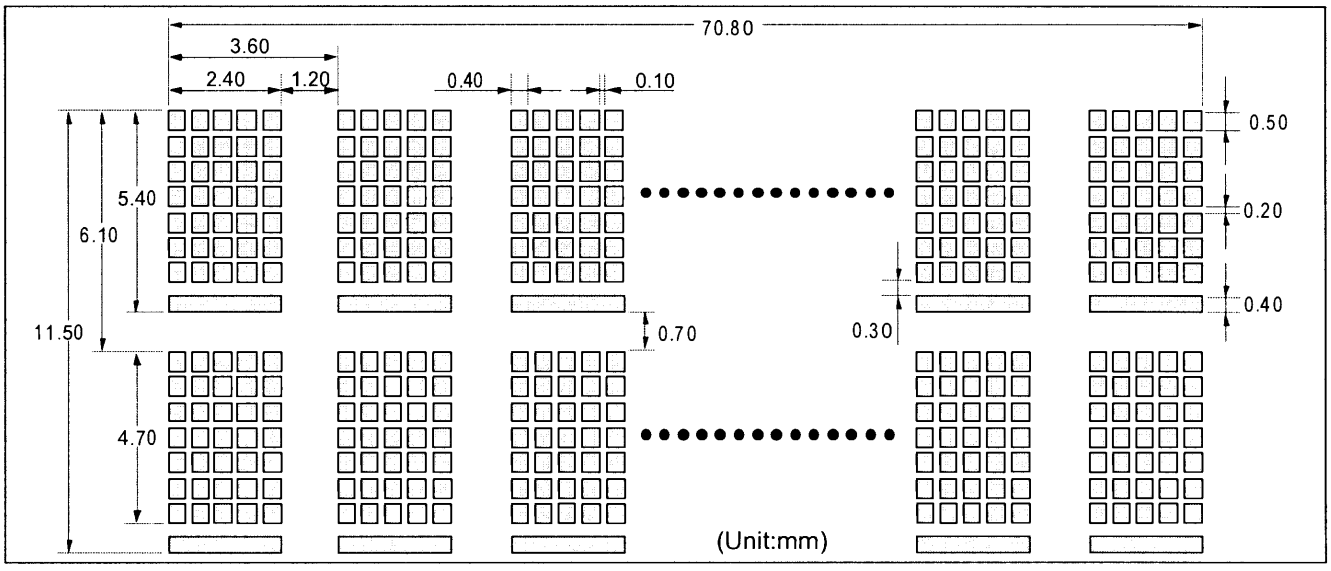


Fig-7. Pattern Details

5. FUNCTION DESCRIPTIONS

5.1 Registers in VFD Controller

The VFD controller has two 8-bit registers, an instruction register (IR) and a data register (DR). IR stores instruction codes, such as display clear and cursor shift, and address information for DD-RAM and CG-RAM. The IR can only be written from the host MPU. DR temporarily stores data to be written into DD-RAM or CG-RAM and temporarily stores data to be read from DD-RAM or CG-RAM. Data written into the DR from the MPU is automatically written into DD-RAM or CG-RAM by an internal operation. The DR is also used for data storage when reading data from DD-RAM or CG-RAM. When address information is written into the IR, data is read and then stored into the DR from DD-RAM or CG-RAM by internal operation. Data transfer between MPU is then completed when the MPU reads the DR. After the read, data in DD-RAM or CG-RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (See Table_9).

Table_9. Register Selection

RS	R/W	
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DDRAM or CGRAM)
1	1	DR read as an internal operation (DDRAM or CGRAM to DR)

5.1.1 Address Counter (ACC)

The address counter (ACC) assigns addresses to both DD-RAM and CG-RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the ACC. Selection of either DD-RAM or CG-RAM is also determined concurrently by the instruction. After writing into (reading from) DD-RAM or CG-RAM, the ACC is automatically incremented by 1 (decremented by 1). The ACC contents are then output to DB0 to DB6 when RS = 0 and R/W = 1 (See table_9).

5.1.2 Display Data RAM (DD-RAM)

Display data RAM (DD-RAM) stores display data represented in 8-bit character codes. The area in DD-RAM that is not used for display can be used as general data RAM. See Table_10 for the relationships between DD-RAM addresses and positions on the VFD.

Table_10. Relation between Digit Position and DD-RAM data

	Left End	2nd Column	3rd Column	.....	19th Column	Right End
1st Row	00 Hex	01 Hex	02 Hex	.....	12 Hex	13 Hex
2nd Row	40 Hex	41 Hex	42 Hex	.....	52 Hex	53 Hex

5.1.3 Character Generator ROM (CG-ROM)

The CG-ROM generates character patterns of 5x7 dots from 8-bit character codes (Table_11). It can generate 240 kinds of 5x7 dot character patterns. The character fonts are shown on the following page. The character codes 00H to 0FH are allocated to the CG-RAM.

5.1.4 Character Generator RAM (CG-RAM)

In the character generator RAM (CG-RAM), the user can rewrite character patterns by program. For 5x7 dots and cursor, eight patterns can be written. Write into DD-RAM the character codes at the addresses shown as the left column of Table_11 to show the character patterns stored in CG-RAM. See Table_12 for the relationship between CG-RAM addresses and data and display patterns and refer to Fig-8 for dot assignment of VFD. Areas that are not used for display can be used as general data RAM.

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
36				

Fig-8. Dot Assignment

Table-11. Characters Font Table (CG-ROM) and CG-RAM codes

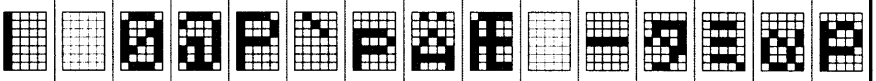
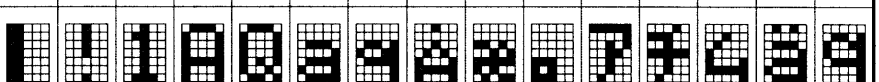
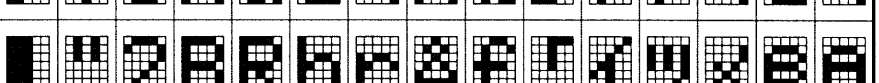
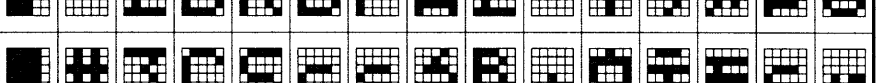
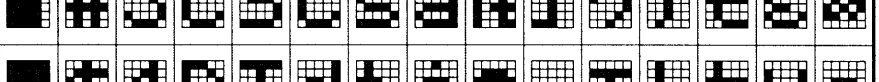
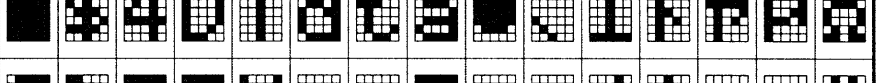
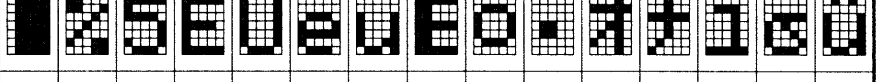
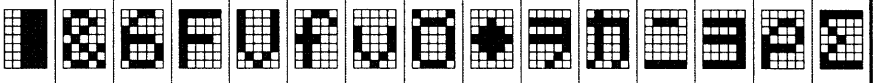
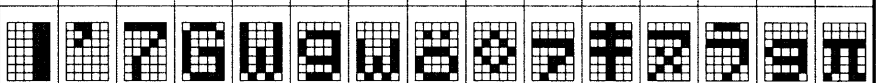
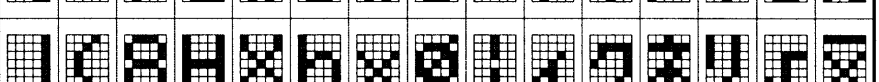
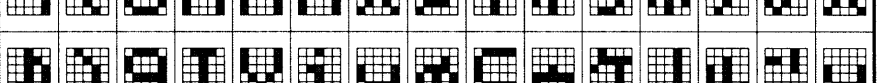
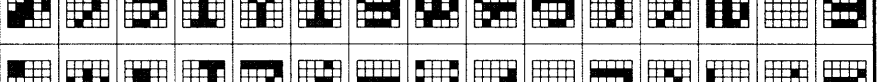
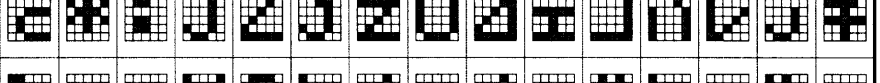
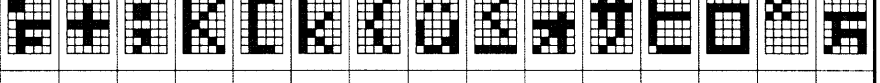
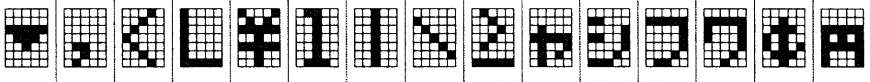
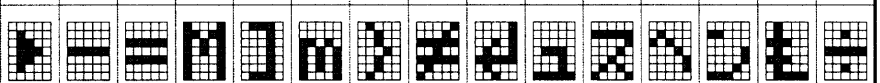
Upper bits / Lower bits	DB7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	DB6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	DB5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	DB4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DB3 DB2 DB1 DB0		**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
0 0 0 0	**0**	CG-RAM (1)															
0 0 0 1	**1**	CG-RAM (2)															
0 0 1 0	**2**	CG-RAM (3)															
0 0 1 1	**3**	CG-RAM] (4)															
0 1 0 0	**4**	CG-RAM (5)															
0 1 0 1	**5**	CG-RAM (6)															
0 1 1 0	**6**	CG-RAM (7)															
0 1 1 1	**7**	CG-RAM (8)															
1 0 0 0	**8**	CG-RAM (1)															
1 0 0 1	**9**	CG-RAM (2)															
1 0 1 0	**A**	CG-RAM (3)															
1 0 1 1	**B**	CG-RAM] (4)															
1 1 0 0	**C**	CG-RAM (5)															
1 1 0 1	**D**	CG-RAM (6)															
1 1 1 0	**E**	CG-RAM (7)															
1 1 1 1	**F**	CG-RAM (8)															

Table-12. Relationship between CG-RAM Addresses, Character Codes(DD-RAM) and 5x7 (with Cursor) Dot Character Patterns (CG-RAM data)

Character Codes (DD-RAM data)								CG-RAM Address						Character Patterns (CG-RAM data)								
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A5	A4	A3	A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	1	2	3	4	5	Character Pattern(1)
											0	0	1	x	x	x	6	7	8	9	10	
											0	1	0	x	x	x	11	12	13	14	15	
											0	1	1	x	x	x	16	17	18	19	20	
											1	0	0	x	x	x	21	22	23	24	25	
											1	0	1	x	x	x	26	27	28	29	30	
											1	1	0	x	x	x	31	32	33	34	35	
											1	1	1	x	x	x	36	x	x	x	x	Cursor position
0	0	0	0	x	0	0	1	0	0	1	0	0	0	x	x	x	1	2	3	4	5	Character Pattern(2)
											0	0	1	x	x	x	6	7	8	9	10	
											0	1	0	x	x	x	11	12	13	14	15	
											0	1	1	x	x	x	16	17	18	19	20	
											1	0	0	x	x	x	21	22	23	24	25	
											1	0	1	x	x	x	26	27	28	29	30	
											1	1	0	x	x	x	31	32	33	34	35	
											1	1	1	x	x	x	36	x	x	x	x	Cursor position
0	0	0	0	x	0	1	0	0	1	0	0	0	0	x	x	x	1	2	3	4	5	
											0	0	1	x	x	x	6	7	8	9	10	
											0	1	0	x	x	x	11	12	13	14	15	
											0	1	1	x	x	x	16	17	18	19		
0	0	0	0	x	1	1	1	1	1	1	1	0	1	x	x	x	26	27	28	29	30	
											1	1	0	x	x	x	31	32	33	34	35	
											1	1	1	x	x	x	36	x	x	x	x	

Notes: 1. Character code bits 0 to 2 correspond to CG-RAM address bits 3 to 5 (3 bits : 8 types).
2. CG-RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.
If bit 4 of the 8th line data is 1, 1 bit will light up the cursor regardless of the cursor presence.
3. Character pattern row positions correspond to CG-RAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table-12, CG-RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CG-RAM data corresponds to display selection and 0 to non-selection.

"**x**" Indicates no effect (Don't care)

5.2 Data transfer

When data written, data can be input when strobe goes "0". 1st byte is Start byte, register to select IR or DR by RS (bit6) bit and data write or read by R/W (bit5=0) in this byte.
And next byte is instruction byte. (See Fig-9)
When data is read, to read the Busy flag + Address counter (AC6 to AC0) or to read the data which was written in DD-RAM or CG-RAM is chosen by the start byte to input first.
Data is output at the falling edge of the shift clock (See Fig-10 and Fig-11).

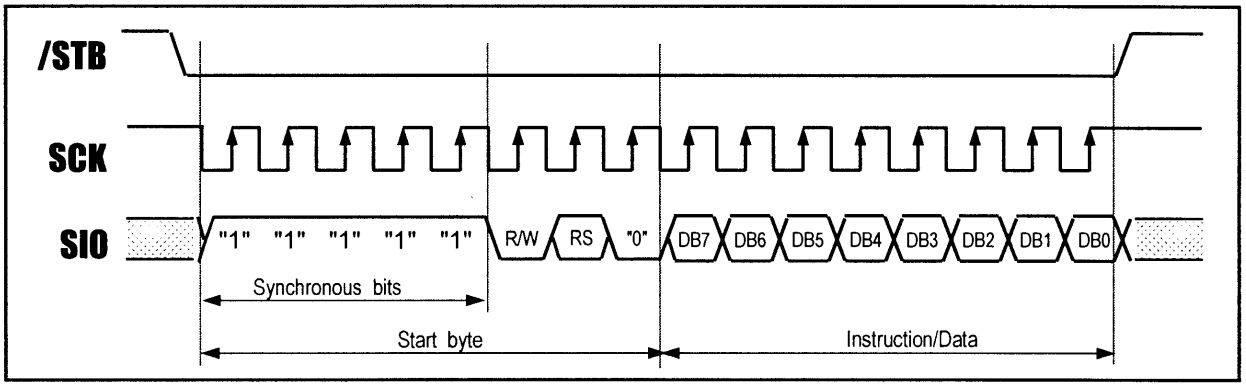


Fig-9. Serial Data Transfer (Data Write)

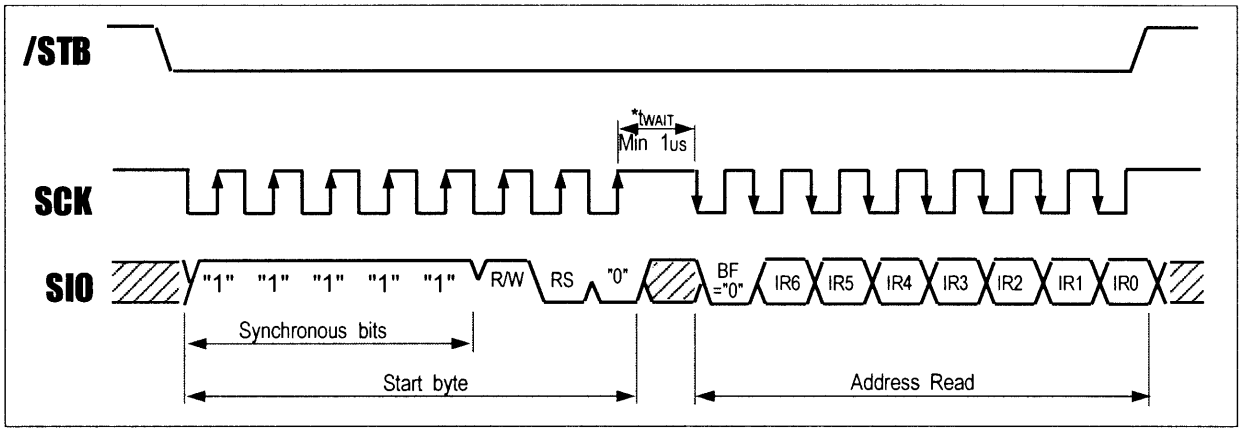


Fig-10. Serial Data Transfer (Address Read)

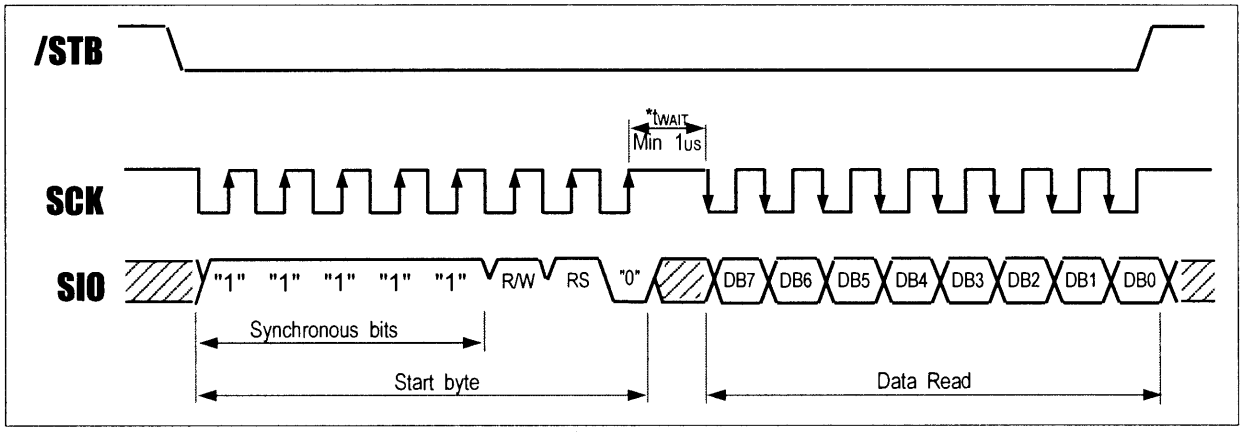


Fig-11. Serial Data Transfer (Data Read)

*Note) tWAIT: Wait time

5.3 Reset Function

5.3.1 Power-on reset

An internal reset circuit automatically initializes the module when the power is turned on. The following instructions are executed during the initialization.

1) Display clear
   Fill the DD-RAM with 20H (Space Code)
2) Set the address counter to 00H
   Set the address counter (ACC) to point DD-RAM.
3) Display on/off control:
   D = 0 ; Display off
   C = 0 ; Cursor off
   B = 0 ; Blinking off
4) Entry mode set:
   I/D = 1 ; Increment by 1
   S = 0 ; No shift
5) Function Set
   N = 1 ; 2-line display
   BR0 = BR1 =0 ; Brightness = 100%

6.INSTRUCTIONS

6.1 Outline

Only the instruction register (IR) and the data register (DR) of the VFD controller can be controlled by the user's MPU. Before starting the internal operation of the controller, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the controller is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/write signal (R/W), and the data bus (DB0 to DB7), make up the controller instructions (See Table_14).
There are four categories of instructions that:

* Designate controller functions, such as display format, data length, etc.
* Set internal RAM addresses
* Perform data transfer with internal RAM
* Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most.
However, auto-increment by 1 (or auto-decrement by 1) of internal RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

Table-14. Instruction Set

Instruction	CODE										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display Clear	0	0	0	0	0	0	0	0	0	1	Clears all display and sets DD-RAM address 0 in address counter.
Cursor Home	0	0	0	0	0	0	0	0	1	x	Sets DDRAM address 0 in ACC. Also returns the display being shifted to the original position. DD-RAM contents remain unchanged.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor direction and specifies display shift. These operations are performed during writing/reading data.
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF(D), cursor ON/OFF(C), cursor blink of character position(B)
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Shifts display or cursor, keeping DD-RAM contents.
Function Set	0	0	0	0	1	IF	N	x	BR1	BR0	Sets data length(IF), number of display lines(N), Set brightness level(BR1,BR0)
CGRAM Address Setting	0	0	0	1	ACG						Sets the CG-RAM address.
DDRAM Address Setting	0	0	1	ADD							Sets the DD-RAM address.
Busy Flag & Address Reading	0	1	BF	ACC							Read busy flag(BF) and address counter (ACC).
Data Writing to CG or DDRAM	1	0	Data writing								Writes data into CG-RAM or DDRAM.
Data Reading from CG or DDRAM	1	1	Data reading								Reads data from CG-RAM or DDRAM.
* NOTE	I/D = 1 : Increment I/D = 0 : Decrement S = 1 : Display shift enabled S = 0 : Cursor shift enabled S/C = 1 : Display shift S/C = 0 : Cursor move R/L = 1 : Shift to the right R/L = 0 : Shift to the left IF = 1 : 8bits IF = 0 : 4bits N = 1 : 2 Lines display N = 0 : 1 Line display BR1, BR0 = 00 : 100% 01 : 75% 10 : 50% 11 : 25% BF = 1 : Busy (Internally operating) BF = 0 : Not busy (Instruction acceptable) x : Don't Care										[Abbreviation] DD-RAM : Display Data RAM CG-RAM : Character Generator RAM ACG : CG-RAM Address ADD : DD-RAM Address ACC : Address Counter

6.2 Instruction Descriptions

6.2.1 Display Clear

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	01H

RS = 0, R/W = 0

This instruction
(1) Fills all locations in the display data RAM (DD-RAM) with 20H (Blank-character).
(2) Clears the contents of the address counter (ACC) to 00H.
(3) Sets the display for zero character shift (returns original position).
(4) Sets the address counter (ACC) to point to the DD-RAM.
(5) If the cursor is displayed, moves the cursor to the left most character in the top line (upper line).
(6) Sets the address counter (ACC) to increment on the each access of DD-RAM or CG-RAM.

6.2.2 Cursor Home

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	x	02H to 03H

RS = 0, R/W = 0 x : Don't care

This instruction
(1) Clears the contents of the address counter (ACC) to 00H.
(2) Sets the address counter (ACC) to point to the DD-RAM.
(3) Sets the display for zero character shift (returns original position).
(4) If the cursor is displayed, moves the left most character in the top line (upper line).

6.2.3 Entry Mode Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	I/D	S	04H to 07H

RS = 0, R/W = 0

The I/D bit selects the way in which the contents of the address counter (ACC) are modified after every access to DD-RAM or CG-RAM.
I/D = 1 : The address counter (ACC) is increased.
I/D = 0 : The address counter (ACC) is decreased.

The S bit enables display shift, instead of cursor shift, after each write or read to the DD-RAM.
S = 1 : Display shift enabled.
S = 0 : Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor.
For example, if S=0 and I/D=1, the cursor would shift one character to the right after a MPU writes to DD-RAM. However if S=1 and I/D=1, the display would shift one character to the left and the cursor would maintain its position on the panel.

The cursor will already be shifted in the direction selected by I/D during reads of the DD-RAM, irrespective of the value of S. Similarly reading and writing the CG-RAM always shift the cursor. Also both lines are shifted simultaneously.

Table_15. Cursor move and Display shift by the "Entry Mode Set"

I/D	S	After writing DD-RAM data	After reading DD-RAM data
0	0	The cursor moves one character to the left.	The cursor moves one character to the left.
1	0	The cursor moves one character to the right.	The cursor moves one character to the right.
0	1	The display shifts one character to the right without cursor's move.	The cursor moves one character to the left.
1	1	The display shifts one character to the left without cursor's move.	The cursor moves one character to the right.

6.2.4 Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	D	C	B	08H to 0FH

RS = 0, R/W = 0

This instruction controls various features of the display.

D = 1 : Display on, D = 0 : Display off.
C = 1 : Cursor on, C = 0 : Cursor off.
B = 1 : Blinking on, B = 0 : Blinking off

(Blinking is achieved by alternating between a normal and all on display of a character. The cursor blinks with a frequency of about 1.0 Hz and DUTY 50%.)

6.2.5 Cursor/Display Shift

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	S/C	R/L	x	x	10H to 1FH (x : Don't care)

RS = 0, R/W = 0

This instruction shifts the display and/or moves the cursor, one character to the left or right, without reading or writing DD-RAM.

The S/C bit selects movement of the cursor or movement of both the cursor and the display.

S/C = 1 : Shift both cursor and display
S/C = 0 : Shift cursor only

The R/L bit selects left ward or right ward movement of the display and/or cursor.

R/L = 1 : Shift one character right
R/L = 0 : Shift one character left

Table_16. Cursor/Display shift

S/C	R/L	Cursor shift	Display shift
0	0	Move one character to the left	No shift
0	1	Move one character to the right	No shift
1	0	Shift one character to the left with display	Shift one character to the left
1	1	Shift one character to the right with display	Shift one character to the right

6.2.6 Function Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	1	N	x	BR1	BR0	20H to 3FH

RS = 0, R/W = 0 x : Don't care

This instruction sets the number of display line and brightness control.
This instruction initializes the system, and must be the first instruction executed after power-on.

The N bit selects between 1-line or 2-line display.
N = 1 : Select 2 line display (Using anode output A1 to A80)
N = 0 : Select 1 line display (Using anode output A1 to A40. A41 to A80 fixed Low level.)
BR1, BR0 flag is control to brightness of VFD to modulate pulse width of Anode output as follows.

BR1	BR0	Brightness
0	0	100 %
0	1	75 %
1	0	50 %
1	1	25 %

6.2.7 Set CG-RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	ACG						40H to 7FH

RS = 0, R/W = 0

This instruction
(1) Load a new 6-bit address into the address counter (ACC).
(2) Sets the address counter (ACC) to address CG-RAM.

Once "Set CG-RAM Address" has been executed, the contents of the address counter (ACC) will be automatically modified after every access of CG-RAM, as determined by the "Entry Mode Set" instruction. The active width of the address counter (ACC), when it is addressing CG-RAM, is 6 bits, so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CG-RAM.

6.2.8 Set DD-RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	ADD							80H to A7H (1-Line) C0H to E7H (2-Line)

RS = 0, R/W = 0

This instruction
(1) Loads a new 7-bit address into the address counter (ACC).
(2) Sets the address counter (ACC) to point to the DD-RAM.

Once the "Set DD-RAM Address" instruction has been executed, the contents of the address counter (ACC) will be automatically modified after each access of DD-RAM, as selected by the "Entry Mode Set" instruction.

Table_17. Valid DD-RAM address Ranges

	Number of Character	Address Range
1st line	40	00H to 27H
2nd line	40	40H to 67H

6.2.9 Read Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF=0	ACC						

RS = 0, R/W = 1

The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter (ACC) in binary AAAAAAA is read out. This address counter (ACC) is used by both CG-RAM and DD-RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CG-RAM address and set DD-RAM address.

6.2.10 Write Data to CG or DD-RAM

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Data Write								00H to FFH

RS = 1, R/W = 0

This instruction writes 8-bit binary data (DB7 to DB0) into CG-RAM or DD-RAM.
To write into CG-RAM or DD-RAM is determined by the previous specification of the CG-RAM or DD-RAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.
When data is written to the CG-RAM, the DB7, DB6 and DB5 bits are not displayed as characters.

6.2.11 Read Data from CG or DD-RAM

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Data Read							

RS = 1, R/W = 1

This instruction reads 8-bit binary data (DB7 to DB0) from CG-RAM or DD-RAM.

The previous designation determines whether CG-RAM or DD-RAM is to be read.
Before entering this read instruction, either CG-RAM or DD-RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD-RAM).
The operation of the cursor shift instruction is the same as the set DD-RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1.

Note : The address counter (ACC) is automatically increased or decreased by 1 after the write instructions to CG-RAM or DD-RAM are executed. The RAM data selected by the ACC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD-RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

7.OPERATING RECOMMENDATIONS

7.1 Avoid applying excessive shock or vibration beyond the specification for the VFD module.

7.2 Since VFDs are made of glass material, careful handling is required.
i.e. Direct impact with hard material to the glass surface(especially exhaust tip) may crack the glass.

7.3 When mounting the VFD module to your system, leave a slight gap between the VFD glass and your front panel.
The module should be mounted without stress to avoid flexing of the PCB.

7.4 Avoid plugging or unplugging the interface connection with the power on, otherwise it may cause the severe damage to input circuitry.

7.5 Exceeding any of maximum ratings may cause the permanent damage.

7.6 Since the VFD modules contain high voltage source, careful handling is required during powered on.

7.7 When the power is turned off, the capacitor does not discharge immediately.
The high voltage applied to the VFD must not contact to the ICs. And the short-circuit of mounted components on PCB within 30 seconds after power-off may cause damage to those.

7.8 The power supply must be capable of providing at least 3 times the rated current, because the surge current can be more than 3 times the specified current consumption when the power is turned on.

7.9 Avoid using the module where excessive noise interference is expected. Noise may affects the interface signal and causes improper operation. And it is important to keep the length of the interface cable less than 50cm.

7.10 Since all VFD modules contain C-MOS ICs, anti-static handling procedures are always required.