Specification

資料中心參考文件用章
For Reference Only
2017.05.23
聯合聚晶股份有限公司
Integrated Solution Technology, Inc

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
Research & Development	michael 05/23/2017	Bonnie Lee 05/23/2017	Bonnie Lee 05/23/2017

Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁
Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
P001	-	New release	E08140001	Plato	2014/08/04
P002	P4	Add VDDIO description	E10140004	Michael	2014/10/13
	P46	Updated “Power Supply Applications”			
	P47~48	Updated “Reference Applications”			
P003	P46	Updated “Power Supply Applications”	E10140018	Michael	2014/10/23
	P47~48	Updated “REFERENCE APPLICATIONS”			
P004	P5	Updated pin description of IIC	E11140001	Michael	2014/11/03
001	P22	Delete “Temperature sensor adjust” & “Frame rate compensation”	E03150009	Jonathan	2015/03/27
	P30~34	Updated “Temperature Sensor”			
		Removed ”Preliminary”			
002	P24	VCK frequency calculate	E04150004	Plato	2015/04/09
	P29	Add BT and PVC description			
	P38~P41	Add Power sequence and Sleep Sequence			
	P49~P53	Add VDDL=1.5V~1.8V Application			
003	P2~4,6,8	Add VFSOURCE	E04150010	michael	2015/04/22
	P22	Add “Efuse mode” command Add “PVC adjusting” command Add “PVC_ADJ fuse enable” command Add “Efuse program enable” command Add “Efuse program start” command			
	P27	Updated PVC voltage formula			
	P36~37	Add “Efuse mode” detail Add “PVC adjusting” detail			

		Add “PVC_ADJ fuse enable” detail Add “Efuse program enable” detail Add “Efuse program start” detail			
	P43	Add VFSOURCE into DC Characteristics table	E04150010	michael	2015/04/22
	P54~55	Add VFSOURCE into diagram of MPU interfaces			
004	P7	Change Bump Height from 9um to 12um.	E05150007	michael	2015/05/26
005	P49	CP[2:0]/CP[1:0]/CP[0] changed to CF[2:0]/ CF[1:0]/CF[0]; PVC must changed to PVCMAX; Updated BT1-0 content. Updated VDLS value when VD[1:0]=01B	E09150003	michael	2015/09/16
006	P7	Change Bump Height from 12um to 9um.	E10160003	michael	2016/10/06
007	P46	Static DC add " Ta=25℃"condition.	E12160002	Plato	2016/12/02
008	P2, P44	Change Operation temperature range from -30~80℃ to -40~90℃	E04170001	Plato	2017/04/06
009	P44 P45	Updated EFUSE power Delete output current; Updated LCD driver ON resistance Updated SNOW pattern current	E04170005	michael	2017/04/24
	P46~P49	Updated AC characteristics			
010	P24, P51	Add using 1.8V regulator procedure	E05170011	michael	2017/05/23

接續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

128SEG x 128COM ULTRA LOW POWER STN-LCD GRAPHICS DISPLAY CONTROLLER & DRIVER

The IST7920 is a single chip STN-LCD controller & driver for graphic dot-matrix display. This chip integrates STN-LCD graphic display controller, display data RAM, oscillator circuits, power circuits and 128 segments x 128 commons driver outputs. It can be directly interfaced with 8080/ 6800-series 8-bit microprocessor, or various serial interfaces. The graphic display data can be stored in the on-chip 1-1 mapping display RAM of 128x128 bits and drive up to 128x128 dot matrix STN-LCD panel.

This chip is especially designed for ultra low power consumption applications, like Electronic Shelf Label (ESL) and watch, which power is supplied by 3V button cells. In addition, because it integrates all the required power supply circuits for driving the STN-LCD panel, like high efficiency voltage converter, high-accuracy voltage regulator, voltage follower circuits and OP-Amps, it is possible to make the lowest power consumption with the fewest external components for high performance portable applications.

FEATURES

Power Supply
- Logic Power : 1.8 ~ 3.6V (VDD1)
- 1.5 ~ 3.6V (VDDL/VDDIO)
- Analog Power : 1.8 ~ 3.6V (VDD2/VDD3)
- Internal LCD Power: 13.5V (max) (PVC–VSS1)
- external LCD Power: 13.5V (max) (PVC–VSS1)
- EFUSE supply: 8V (VFSOURCE)

Display Driver Output Circuits
- 128 segment outputs
- 128 common outputs
- Display Duty = 1/16~ 1/128
- Applicable Bias: 1/8 ~ 1/15

On-chip Display Data RAM
- RAM size : 128X128 = 16,384 bits

Built-in Analog Circuit
- Ultra low display power consumption
- On-chip oscillator circuit for display clock (external clock can also be used)
- High performance voltage converter
- High accuracy reference voltage generator
- Electronic contrast control (256 steps)
- Embedded Voltage regulator
- Embedded Voltage follow.

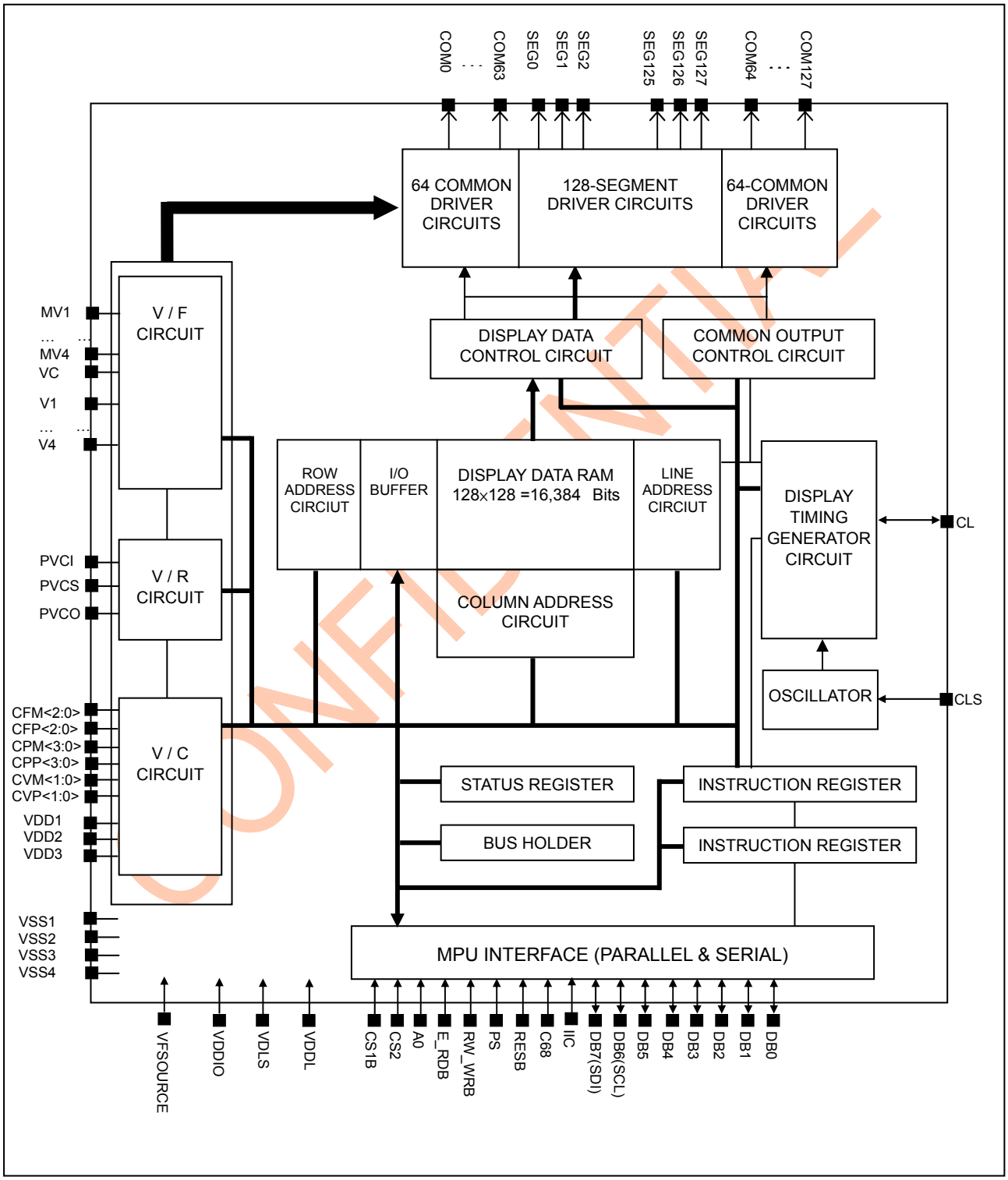
Microprocessor Interface
- High-speed 8080/6800-series 8-bit parallel bi-directional interface
- Serial 3/4 line Write/Read interface
- IIC Write/Read interface

Various Function Set
- Display On/Off control
- Set display starting line,
- Set row/column address
- Software reset
- Read Status
- Reverse display
- Select Bias
- Set Duty
- COM/SEG output direction control
- Display power control
- LCD Contrast control

Operating Temperatures
- Wide range of operating temperatures from -40℃ to 90℃

Package Type
- COG(Gold-bumped bared chip)

BLOCK DIAGRAM



PAD DESCRIPTION

Power Supply

Name	I/O	Description
VDDL	Power Supply	Logic power supply
VDDIO	Power Supply	IO power supply
VDD1 VDD2 VDD3	Power Supply	Power source
VSS1 VSS2 VSS3 VSS4	Power Supply	Ground
VFSOURCE	Power Supply	EFUSE power supply，if not using, keep it open.
CFM<2:0> CFP<2:0>	I/O	Driver voltage generator peripheral pins. Connect external capacitor between CFM and CFP.
CPM<3:0> CPP<3:0>	I/O	PVC generator peripheral pins. Connect external capacitor between CPM and CPP.
CVM<1:0> CVP<1:0>	I/O	VDDL generator peripheral pins. Connect external capacitor between CVM and CVP.

System Control

Name	I/O	Description
CLS	I	Built-in oscillator circuit enable / disable select pin - CLS = “H” : enable (this pin is used together with digital command) - CLS = “L” : disable (external display clock input through CL pin)
CL	I/O	External clock input pin, It must fix to VSS1 or VDD1 when CLS is “H”
VDLS	I	External VDDL enable / disable select pin - VDLS = “H” : enable (this pin is used together with digital command) - VDLS = “L” : disable (this pin is used together with digital command)

Micro-Controller Interface

Name	I/O	Description						
RESB	I	Hardware Reset input pin When RESB is “L”, initialization is executed.						
PS	I	Parallel / serial data input select input, and IIC must set to “H”						
		PS	Interface mode	Chip select	Data / instruction	Data	Read / Write	Serial clock
		H	Parallel	CS1B, CS2	A0	DB0 to DB7	E_RDB RW_WRB	--
		L	Spi3/spi4	CS1B, CS2	-	SDI (DB7)	Write/Read	SCL (DB6)

<table>
<tr><td></td><td></td><td colspan="4"><NOTE> In serial mode, DB0 to DB5 and E_RDB and RW_WRB must be fixed to either “H” or “L”. It also define as ID0 when IIC interface (IIC=”L”) is use.</td></tr>
<tr><td>C68</td><td>I</td><td colspan="4">Microprocessor Interface Select input pin in parallel mode(when IIC=”H”,PS=”H”)
- C68 = “H” : 6800-series MPU interface
- C68 = “L” : 8080-series MPU interface
It also define as ID1 when IIC interface(IIC=”L”) is use</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td colspan="4">Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>IIC</td><td>I</td><td colspan="4">IIC mode selection pin. IIC mode is enabled when IIC is “L”.</td></tr>
<tr><td>A0</td><td>I</td><td colspan="4">Register select input pin
- A0 = “H” : DB0 to DB7 are display data
- A0 = “L” : DB0 to DB7 are control data</td></tr>
<tr><td rowspan="4">RW_WRB</td><td rowspan="4">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU Type</td><td>RW_WRB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
- RW = “H” : read
- RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WRB</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.</td></tr>
<tr><td rowspan="4">E_RDB</td><td rowspan="4">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU Type</td><td>E_RDB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
- RW = “H” : When E is “H”, DB0 to DB7 are in an output status.
- RW = “L”: The data on DB0 to DB7 are latched at the falling edge the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RDB</td><td>Read enable clock input pin
When / RDB is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = “L”);
- DB0 to DB5 : high impedance
- DB6 : serial input clock (SCL)
- DB7 : serial input data (SDI)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>VOP</td><td>I/O</td><td colspan="4">Internal voltage reference input/output pin.</td></tr>
<tr><td>PVCI</td><td>I</td><td colspan="4">PVCI is one power of COM and SEG driver.</td></tr>
<tr><td>PVCS</td><td>I</td><td colspan="4">PVCS is the sensor of the PVCI generator.</td></tr>
<tr><td>PVCO</td><td>O</td><td colspan="4">PVCO is the output of PVCI generator.</td></tr>
<tr><td>VC</td><td>O</td><td colspan="4">VC is one power of COM and SEG driver.</td></tr>
<tr><td>V1~V4</td><td>O</td><td colspan="4">Power of COM and SEG driver.</td></tr>
<tr><td>MV1~MV4</td><td>O</td><td colspan="4">Power of COM and SEG driver.</td></tr>
<tr><td>TEST1~2</td><td>I/O</td><td colspan="4">Test pins, must keep them open.</td></tr>
<tr><td>LDR</td><td>I/O</td><td colspan="4">Reserve pin, keep it open.</td></tr>
<tr><td>XTAL1~2</td><td>I/O</td><td colspan="4">Reserve pins, keep them open.</td></tr>
</table>

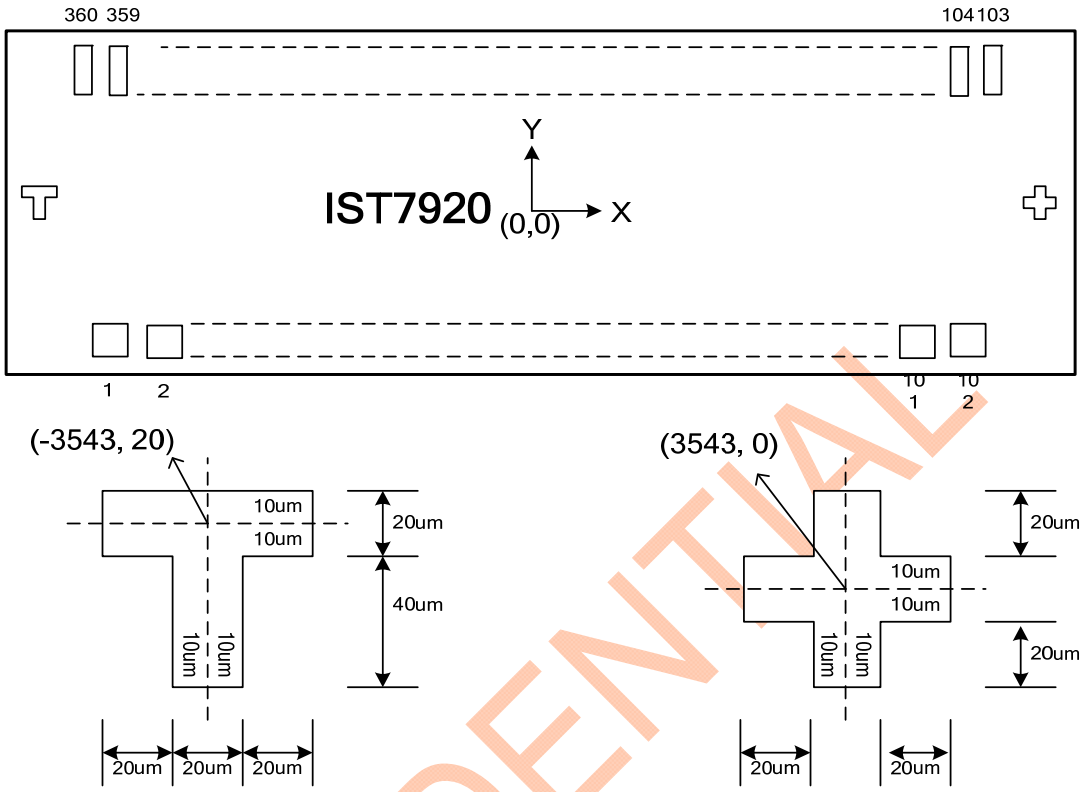
LCD Driver Outputs

Name	I/O	Description
SEG0 ~ SEG127	O	LCD segment driver outputs
COM0 ~ COM127	O	LCD common driver outputs

I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
VDDL, VDD1, VDD3, VSS1, VSS3, VSS4, PVCO, PVCI, PVCS, VDDIO, CFM<2:0>, CFP<2:0>, CPM<3:0>, CPP<3:0>, CVM<1:0>, CVP<1:0>, MV1~MV4, VC, V1~V4, VFSOURCE	<200Ω
VDD2, VSS2,	<100Ω
CS1B, CS2, RW_WRB, E_RDB, A0, DB0~DB7	<1KΩ
RESB	<10KΩ
CL, C68, PS, CLS, IIC, VOP, VDLS	No Limitation

PAD CONFIGURATION



Chip Size	7218 um x 824 um (Exclude Scribe Line)	
Bump Pitch	27um (min)	
Bump Spacing	13um (min)	
Bump Size(X*Y)	40 x 40 um2	Pad No = 1 ~ 102
	14 x 108 um2	Pad No = 103 ~ 360
Bump Height	9um (Typ)	
Chip Thickness	300um (Typ)	

PAD CENTER COORDINATES

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
1	NC	-3535	-371	51	VDD2	-35	-371	101	VDD1	3465	-371
2	VFSOURCE	-3465	-371	52	VDD2	35	-371	102	NC	3535	-371
3	VFSOURCE	-3395	-371	53	VDD2	105	-371	103	NC	3560.5	348
4	VSS1	-3325	-371	54	VDD2	175	-371	104	COM<63>	3533.5	348
5	VDDIO	-3255	-371	55	VDD2	245	-371	105	COM<62>	3506.5	348
6	CS1B	-3185	-371	56	VSS4	315	-371	106	COM<61>	3479.5	348
7	CS2	-3115	-371	57	VSS4	385	-371	107	COM<60>	3452.5	348
8	A0	-3045	-371	58	VSS4	455	-371	108	COM<59>	3425.5	348
9	WRB	-2975	-371	59	VSS3	525	-371	109	COM<58>	3398.5	348
10	RDB	-2905	-371	60	VSS3	595	-371	110	COM<57>	3371.5	348
11	VSS1	-2835	-371	61	VSS2	665	-371	111	COM<56>	3344.5	348
12	VDDIO	-2765	-371	62	VSS2	735	-371	112	COM<55>	3317.5	348
13	DB<0>	-2695	-371	63	VSS2	805	-371	113	COM<54>	3290.5	348
14	DB<1>	-2625	-371	64	VSS2	875	-371	114	COM<53>	3263.5	348
15	DB<2>	-2555	-371	65	VSS2	945	-371	115	COM<52>	3236.5	348
16	DB<3>	-2485	-371	66	MV4	1015	-371	116	COM<51>	3209.5	348
17	DB<4>	-2415	-371	67	MV3	1085	-371	117	COM<50>	3182.5	348
18	DB<5>	-2345	-371	68	MV2	1155	-371	118	COM<49>	3155.5	348
19	DB<6>	-2275	-371	69	MV1	1225	-371	119	COM<48>	3128.5	348
20	DB<7>	-2205	-371	70	VC	1295	-371	120	COM<47>	3101.5	348
21	VDDIO	-2135	-371	71	VC	1365	-371	121	COM<46>	3074.5	348
22	VDDIO	-2065	-371	72	V1	1435	-371	122	COM<45>	3047.5	348
23	VSS1	-1995	-371	73	V2	1505	-371	123	COM<44>	3020.5	348
24	VSS1	-1925	-371	74	V3	1575	-371	124	COM<43>	2993.5	348
25	VSS1	-1855	-371	75	V4	1645	-371	125	COM<42>	2966.5	348
26	VSS1	-1785	-371	76	PVCS	1715	-371	126	COM<41>	2939.5	348
27	VSS1	-1715	-371	77	PVCI	1785	-371	127	COM<40>	2912.5	348
28	C68	-1645	-371	78	PVCI	1855	-371	128	COM<39>	2885.5	348
29	PS	-1575	-371	79	PVCI	1925	-371	129	COM<38>	2858.5	348
30	IIC	-1505	-371	80	PVCO	1995	-371	130	COM<37>	2831.5	348
31	CLS	-1435	-371	81	PVCO	2065	-371	131	COM<36>	2804.5	348
32	CL	-1365	-371	82	CFM<2>	2135	-371	132	COM<35>	2777.5	348
33	VDLS	-1295	-371	83	CFP<2>	2205	-371	133	COM<34>	2750.5	348
34	RESB	-1225	-371	84	CFM<1>	2275	-371	134	COM<33>	2723.5	348
35	TEST1	-1155	-371	85	CFP<1>	2345	-371	135	COM<32>	2696.5	348
36	TEST2	-1085	-371	86	CFM<0>	2415	-371	136	COM<31>	2669.5	348
37	VDDL	-1015	-371	87	CFP<0>	2485	-371	137	COM<30>	2642.5	348
38	VDDL	-945	-371	88	CPM<0>	2555	-371	138	COM<29>	2615.5	348
39	VDDL	-875	-371	89	CPP<0>	2625	-371	139	COM<28>	2588.5	348
40	VDDL	-805	-371	90	CPM<1>	2695	-371	140	COM<27>	2561.5	348
41	VDDL	-735	-371	91	CPP<1>	2765	-371	141	COM<26>	2534.5	348
42	VOP	-665	-371	92	CPM<2>	2835	-371	142	COM<25>	2507.5	348
43	LDR	-595	-371	93	CPP<2>	2905	-371	143	COM<24>	2480.5	348
44	XTAL1	-525	-371	94	CPM<3>	2975	-371	144	COM<23>	2453.5	348
45	XTAL2	-455	-371	95	CPP<3>	3045	-371	145	COM<22>	2426.5	348
46	VDD1	-385	-371	96	PVCI	3115	-371	146	COM<21>	2399.5	348
47	VDD1	-315	-371	97	CVP<1>	3185	-371	147	COM<20>	2372.5	348
48	VDD1	-245	-371	98	CVM<1>	3255	-371	148	COM<19>	2345.5	348
49	VDD3	-175	-371	99	CVP<0>	3325	-371	149	COM<18>	2318.5	348
50	VDD3	-105	-371	100	CVM<0>	3395	-371	150	COM<17>	2291.5	348

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
151	COM<16>	2264.5	348	201	SEG<94>	823.5	348	251	SEG<44>	-526.5	348
152	COM<15>	2237.5	348	202	SEG<93>	796.5	348	252	SEG<43>	-553.5	348
153	COM<14>	2210.5	348	203	SEG<92>	769.5	348	253	SEG<42>	-580.5	348
154	COM<13>	2183.5	348	204	SEG<91>	742.5	348	254	SEG<41>	-607.5	348
155	COM<12>	2156.5	348	205	SEG<90>	715.5	348	255	SEG<40>	-634.5	348
156	COM<11>	2129.5	348	206	SEG<89>	688.5	348	256	SEG<39>	-661.5	348
157	COM<10>	2102.5	348	207	SEG<88>	661.5	348	257	SEG<38>	-688.5	348
158	COM<9>	2075.5	348	208	SEG<87>	634.5	348	258	SEG<37>	-715.5	348
159	COM<8>	2048.5	348	209	SEG<86>	607.5	348	259	SEG<36>	-742.5	348
160	COM<7>	2021.5	348	210	SEG<85>	580.5	348	260	SEG<35>	-769.5	348
161	COM<6>	1994.5	348	211	SEG<84>	553.5	348	261	SEG<34>	-796.5	348
162	COM<5>	1967.5	348	212	SEG<83>	526.5	348	262	SEG<33>	-823.5	348
163	COM<4>	1940.5	348	213	SEG<82>	499.5	348	263	SEG<32>	-850.5	348
164	COM<3>	1913.5	348	214	SEG<81>	472.5	348	264	SEG<31>	-877.5	348
165	COM<2>	1886.5	348	215	SEG<80>	445.5	348	265	SEG<30>	-904.5	348
166	COM<1>	1859.5	348	216	SEG<79>	418.5	348	266	SEG<29>	-931.5	348
167	COM<0>	1832.5	348	217	SEG<78>	391.5	348	267	SEG<28>	-958.5	348
168	SEG<127>	1714.5	348	218	SEG<77>	364.5	348	268	SEG<27>	-985.5	348
169	SEG<126>	1687.5	348	219	SEG<76>	337.5	348	269	SEG<26>	-1012.5	348
170	SEG<125>	1660.5	348	220	SEG<75>	310.5	348	270	SEG<25>	-1039.5	348
171	SEG<124>	1633.5	348	221	SEG<74>	283.5	348	271	SEG<24>	-1066.5	348
172	SEG<123>	1606.5	348	222	SEG<73>	256.5	348	272	SEG<23>	-1093.5	348
173	SEG<122>	1579.5	348	223	SEG<72>	229.5	348	273	SEG<22>	-1120.5	348
174	SEG<121>	1552.5	348	224	SEG<71>	202.5	348	274	SEG<21>	-1147.5	348
175	SEG<120>	1525.5	348	225	SEG<70>	175.5	348	275	SEG<20>	-1174.5	348
176	SEG<119>	1498.5	348	226	SEG<69>	148.5	348	276	SEG<19>	-1201.5	348
177	SEG<118>	1471.5	348	227	SEG<68>	121.5	348	277	SEG<18>	-1228.5	348
178	SEG<117>	1444.5	348	228	SEG<67>	94.5	348	278	SEG<17>	-1255.5	348
179	SEG<116>	1417.5	348	229	SEG<66>	67.5	348	279	SEG<16>	-1282.5	348
180	SEG<115>	1390.5	348	230	SEG<65>	40.5	348	280	SEG<15>	-1309.5	348
181	SEG<114>	1363.5	348	231	SEG<64>	13.5	348	281	SEG<14>	-1336.5	348
182	SEG<113>	1336.5	348	232	SEG<63>	-13.5	348	282	SEG<13>	-1363.5	348
183	SEG<112>	1309.5	348	233	SEG<62>	-40.5	348	283	SEG<12>	-1390.5	348
184	SEG<111>	1282.5	348	234	SEG<61>	-67.5	348	284	SEG<11>	-1417.5	348
185	SEG<110>	1255.5	348	235	SEG<60>	-94.5	348	285	SEG<10>	-1444.5	348
186	SEG<109>	1228.5	348	236	SEG<59>	-121.5	348	286	SEG<9>	-1471.5	348
187	SEG<108>	1201.5	348	237	SEG<58>	-148.5	348	287	SEG<8>	-1498.5	348
188	SEG<107>	1174.5	348	238	SEG<57>	-175.5	348	288	SEG<7>	-1525.5	348
189	SEG<106>	1147.5	348	239	SEG<56>	-202.5	348	289	SEG<6>	-1552.5	348
190	SEG<105>	1120.5	348	240	SEG<55>	-229.5	348	290	SEG<5>	-1579.5	348
191	SEG<104>	1093.5	348	241	SEG<54>	-256.5	348	291	SEG<4>	-1606.5	348
192	SEG<103>	1066.5	348	242	SEG<53>	-283.5	348	292	SEG<3>	-1633.5	348
193	SEG<102>	1039.5	348	243	SEG<52>	-310.5	348	293	SEG<2>	-1660.5	348
194	SEG<101>	1012.5	348	244	SEG<51>	-337.5	348	294	SEG<1>	-1687.5	348
195	SEG<100>	985.5	348	245	SEG<50>	-364.5	348	295	SEG<0>	-1714.5	348
196	SEG<99>	958.5	348	246	SEG<49>	-391.5	348	296	COM<64>	-1832.5	348
197	SEG<98>	931.5	348	247	SEG<48>	-418.5	348	297	COM<65>	-1859.5	348
198	SEG<97>	904.5	348	248	SEG<47>	-445.5	348	298	COM<66>	-1886.5	348
199	SEG<96>	877.5	348	249	SEG<46>	-472.5	348	299	COM<67>	-1913.5	348
200	SEG<95>	850.5	348	250	SEG<45>	-499.5	348	300	COM<68>	-1940.5	348

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
301	COM<69>	-1967.5	348	351	COM<119>	-3317.5	348				
302	COM<70>	-1994.5	348	352	COM<120>	-3344.5	348				
303	COM<71>	-2021.5	348	353	COM<121>	-3371.5	348				
304	COM<72>	-2048.5	348	354	COM<122>	-3398.5	348				
305	COM<73>	-2075.5	348	355	COM<123>	-3425.5	348				
306	COM<74>	-2102.5	348	356	COM<124>	-3452.5	348				
307	COM<75>	-2129.5	348	357	COM<125>	-3479.5	348				
308	COM<76>	-2156.5	348	358	COM<126>	-3506.5	348				
309	COM<77>	-2183.5	348	359	COM<127>	-3533.5	348				
310	COM<78>	-2210.5	348	360	NC	-3560.5	348				
311	COM<79>	-2237.5	348	(END)							
312	COM<80>	-2264.5	348								
313	COM<81>	-2291.5	348								
314	COM<82>	-2318.5	348								
315	COM<83>	-2345.5	348								
316	COM<84>	-2372.5	348								
317	COM<85>	-2399.5	348								
318	COM<86>	-2426.5	348								
319	COM<87>	-2453.5	348								
320	COM<88>	-2480.5	348								
321	COM<89>	-2507.5	348								
322	COM<90>	-2534.5	348								
323	COM<91>	-2561.5	348								
324	COM<92>	-2588.5	348								
325	COM<93>	-2615.5	348								
326	COM<94>	-2642.5	348								
327	COM<95>	-2669.5	348								
328	COM<96>	-2696.5	348								
329	COM<97>	-2723.5	348								
330	COM<98>	-2750.5	348								
331	COM<99>	-2777.5	348								
332	COM<100>	-2804.5	348								
333	COM<101>	-2831.5	348								
334	COM<102>	-2858.5	348								
335	COM<103>	-2885.5	348								
336	COM<104>	-2912.5	348								
337	COM<105>	-2939.5	348								
338	COM<106>	-2966.5	348								
339	COM<107>	-2993.5	348								
340	COM<108>	-3020.5	348								
341	COM<109>	-3047.5	348								
342	COM<110>	-3074.5	348								
343	COM<111>	-3101.5	348								
344	COM<112>	-3128.5	348								
345	COM<113>	-3155.5	348								
346	COM<114>	-3182.5	348								
347	COM<115>	-3209.5	348								
348	COM<116>	-3236.5	348								
349	COM<117>	-3263.5	348								
350	COM<118>	-3290.5	348								

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Chip select control

There are CS1B and CS2 pins for chip selection. The IST7920 can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, A0, E_RDB, and RW_WRB inputs are disabled and DB0 to DB7 are high impedance. In case of serial interface, the internal shift registers and the counter are reset.

MPU Interface types

IST7920 has five types of MPU interface, which are three serial and two parallel interfaces. This parallel or serial interface is determined by IIC, PS, and C68 pin as shown below.

IIC	PS	C68	Type	Interface mode
H	H	H	Parallel	6800-series MPU mode
H	H	L	Parallel	8080-series MPU mod
H	L	H	Serial	3-Line SPI Serial-mode
H	L	L	Serial	4-Line SPI Serial-mode
L	*	*	Serial	IIC Serial-mode

*: PS/C68 is use as ID1/ID0; IIC host can use ID1/ID0 to select difference IIC device.

Parallel Interface (IIC=“H” PS = “H”)

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68. The type of data transfer is determined by signals at A0, E_RDB and RW_WRB as shown below.

C68	CS1B	CS2	A0	E_RDB	RW_WRB	DB0 to DB7	MPU bus
H	CS1B	CS2	A0	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	A0	/RDB	/WRB	DB0 to DB7	8080-series

Common	6800-series		8080-series		Description
A0	E_RDB (E)	RW_WRB (RW)	E_RDB (/RDB)	RW_WRB (/WRB)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (IIC=“H” PS = “L”)

When IIC = “H” PS = “L”, the IST7920 is configured as Serial interface (4-line or 3-line), the serial data can be input through DB7 (SDI) and serial clock can be input through DB6 (SCL).

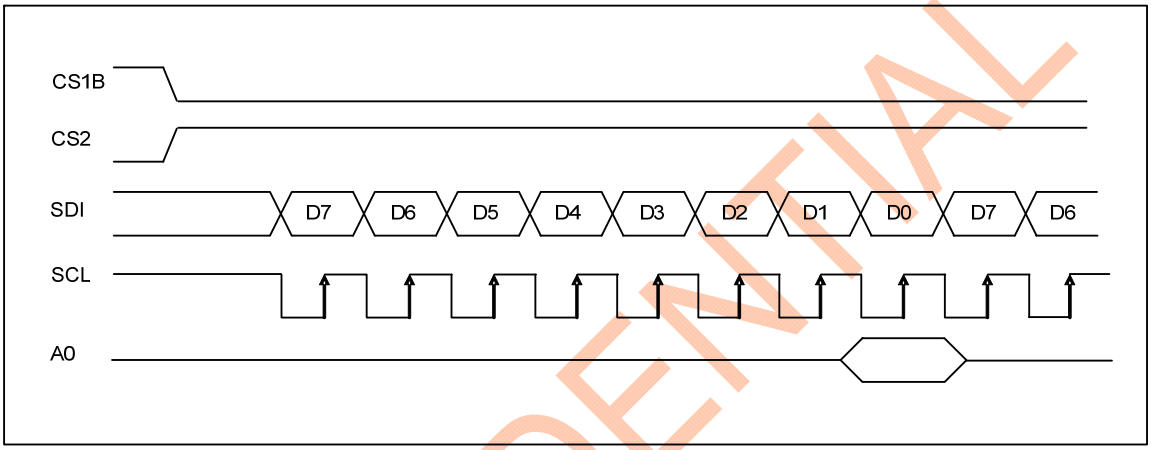
When the chip is not selected, the shift register & serial data counter will be reset and SDI & SCL will also be

disabled internally.

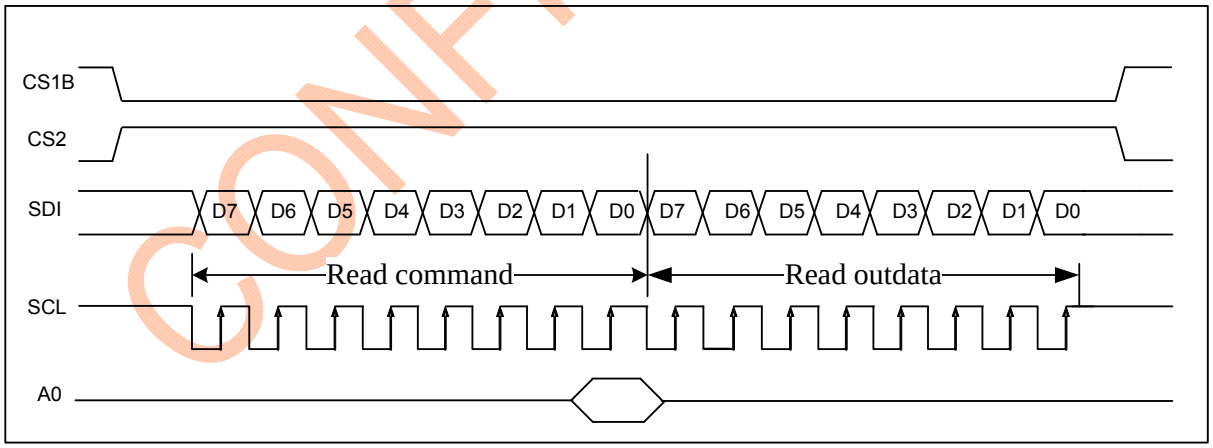
4-Line Serial Interface (IIC="H" PS = "L" C68="L")

When the chip is selected (CS1B="L", CS2="H"), the serial data can be shifted in sequentially at the rising edge of SCL and transferred to 8-bit parallel data internally; at the eighth SCL rising edge, A0 will also be sampled to decide these 8-bit data is interpreted as command or display data.

4-Line Serial Interface Timing



Write operation of 4-Line SPI

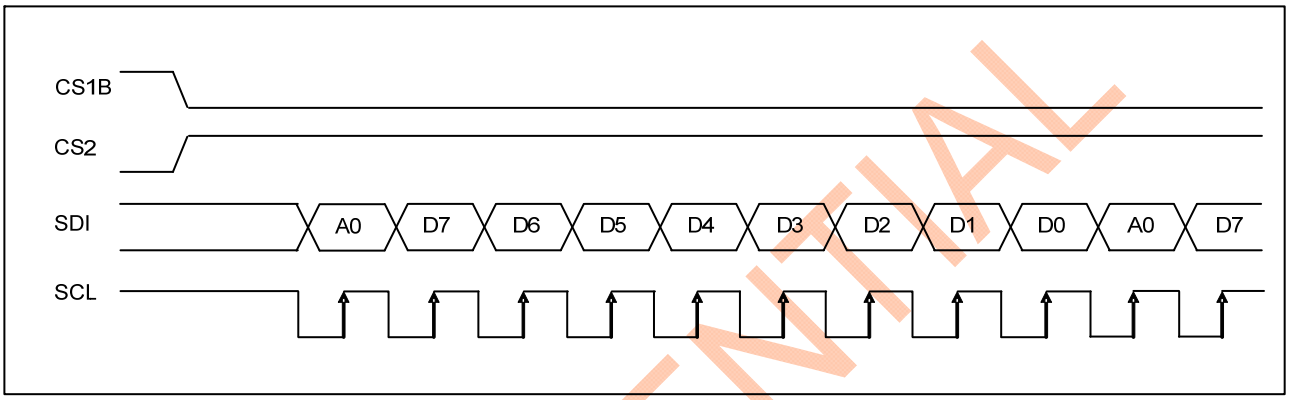


Read operation of 4-Line SPI

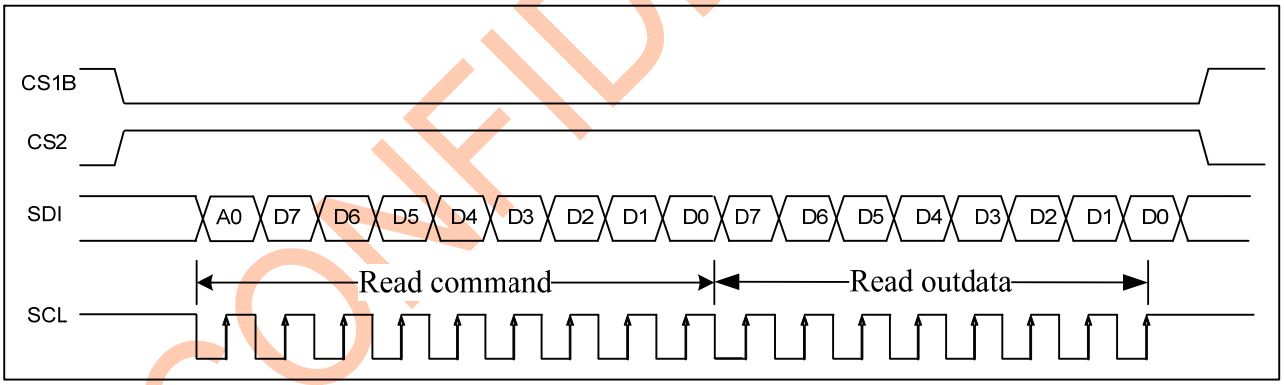
3-Line Serial Interface (IIC="H" PS = "L" C68="H")

In 3-Line interface, A0 signal is not available and the 1st output of SDI will be treated as A0 flag.

3-Line Serial Interface Timing



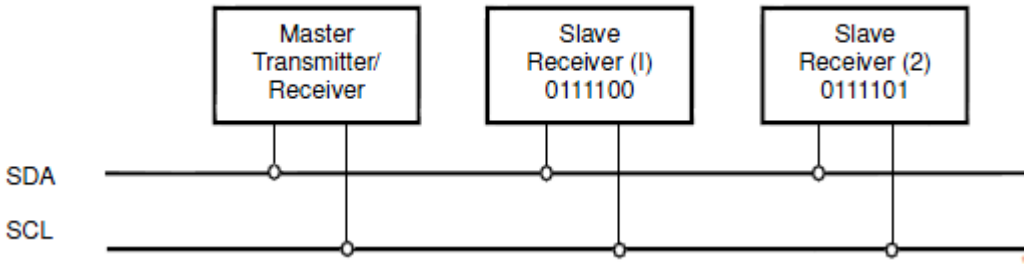
Write operation of 3-Line SPI



Read operation of 3-Line SPI

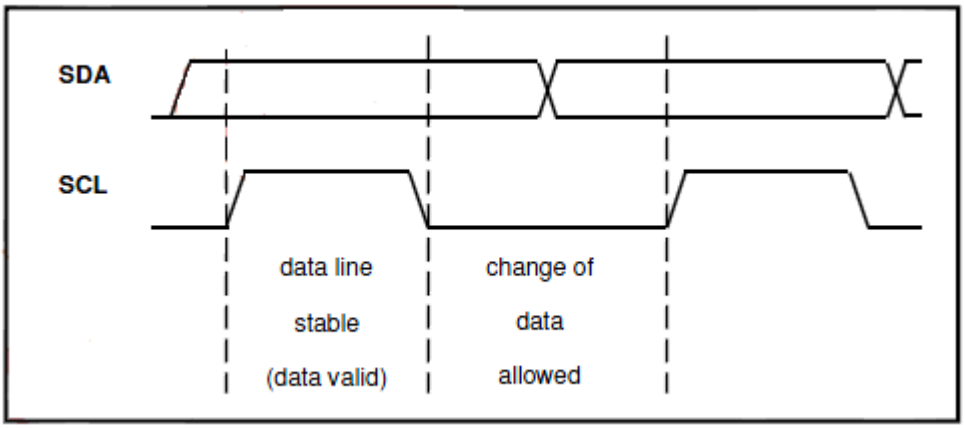
IIC Interface

As 80/68-sreies or 4-line serial interface, The IST7920 also supports standard IIC interface for command & display data communication. The IIC interface is a bi-directional, two-line serial interface, the two lines are a Serial Data line(SDA) and a Serial Clock line(SCL), if MCU(IIC master) IO is open-drain mode, both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.



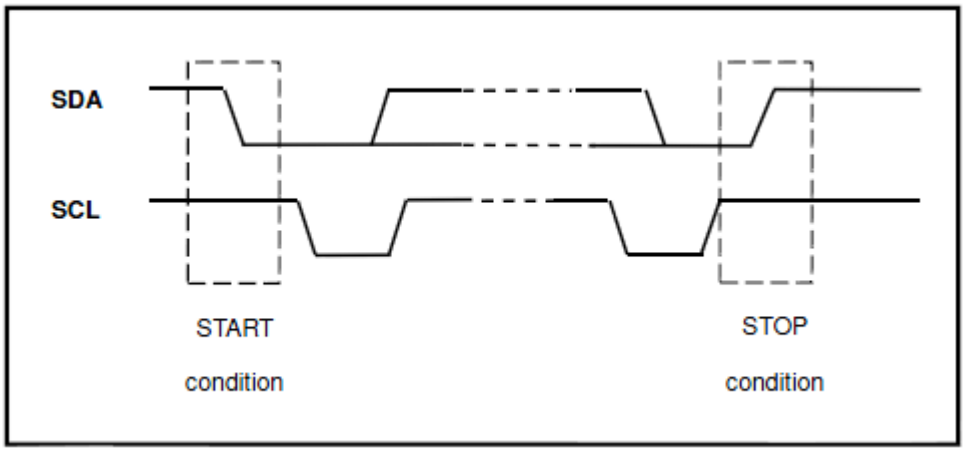
Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes in the data line at this time will be interpreted as a control signal



START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

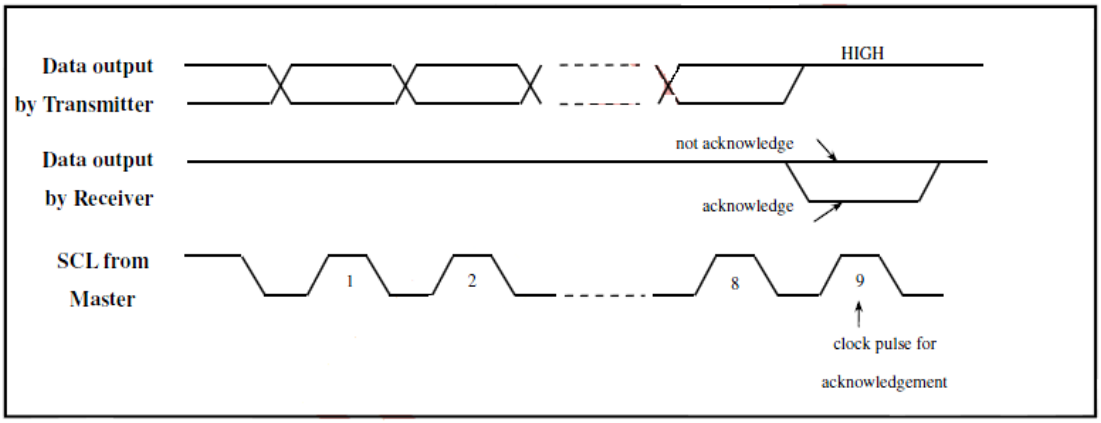


ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledgment bit. The acknowledgment bit is a HIGH signal put on the bus by the transmitter (to release the SDA control and waiting for receiver's acknowledgement), during which time the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledgment after the reception of each byte. A master receiver must also generate an acknowledgment after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge must pull-down the SDA line during the acknowledgment clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledgment related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal and end-of-data to the transmitter by not generating an acknowledgment on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.



IIC Interface Protocol

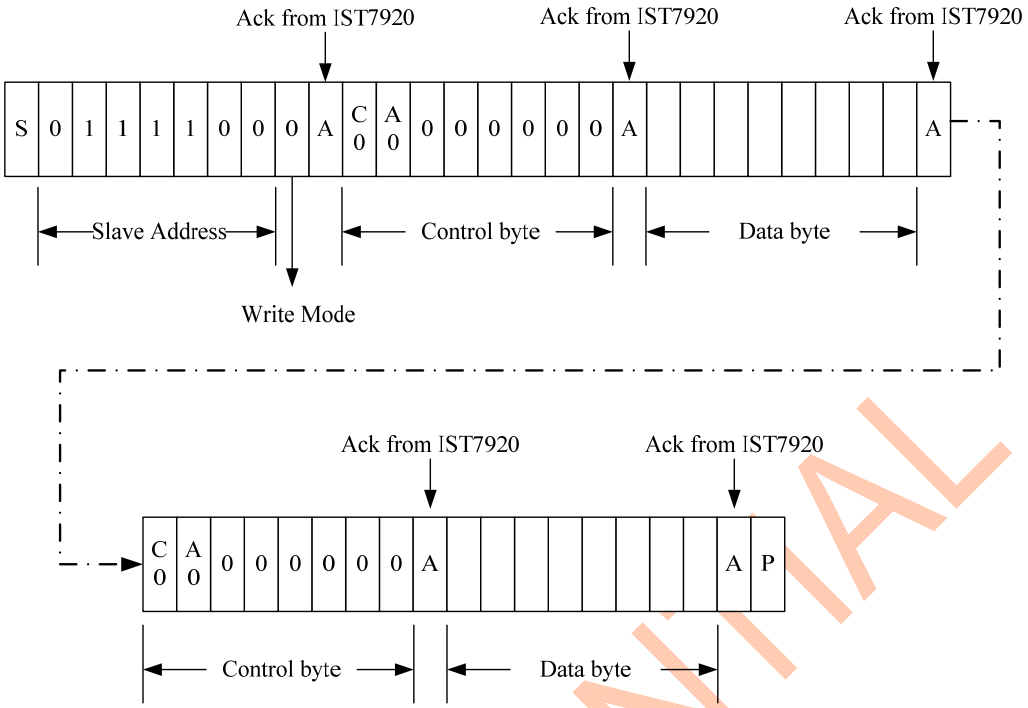
The IIC transmitting is initiated with a START condition (S) from the IIC–bus Master and followed by a slave address. Two 7-bit slave addresses (0111100, 0111101, 0111110, and 0111111) are reserved for the IST7920. The least significant bit of the slave address (ID) is configured by C68 and PS pin to decide is the slave address is 0111100 (C68=0/PS=0) or 0111101 (C68=0/PS=1) or 0111110(C68=1/PS=0) or 0111111(C68=1/PS=1). The 8th bit follows the previous 7-bit address is the data direction bit (R/W) -- '0' indicates Master data transmission (WRITE), '1' indicates Master data request (READ).

WRITE Mode (Master transmits data to Slave, R/W=0)

Write mode includes Slave address byte, control byte & data byte. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines C0 and A0, and a data byte. The control and data bytes are also acknowledged by all addressed slaves on the bus.

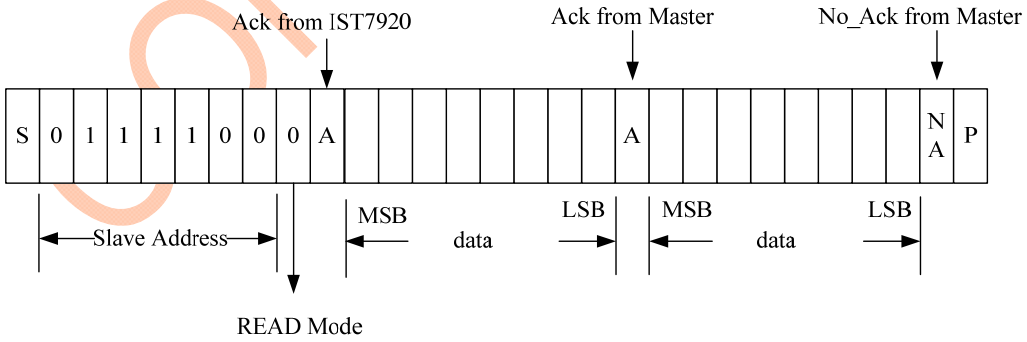
The C0 bit indicates the continuation of the command, please just set C0=1 during the whole Write transmitting period. The A0 bit decides the interpretation of the data byte. If A0 bit is 0, the data byte will be interpreted as command index, if A0 bit is 1, the data byte will be interpreted as command data.

A data transfer is always terminated by a STOP condition (P) generated by the master. However, if master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.



READ Mode (Master requests data from Slave, R/W=1)

At the moment of the first acknowledge, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave transmitter. The first acknowledge is still generated by the slave, but the following data bytes' acknowledgement are generated by Master. The STOP and Re-START conditions are generated by Master. If Master wants to stop the data request, after the last data byte has been received, send a Non-Acknowledge condition (keep SDA at HIGH) and trigger a STOP condition.



Busy Flag

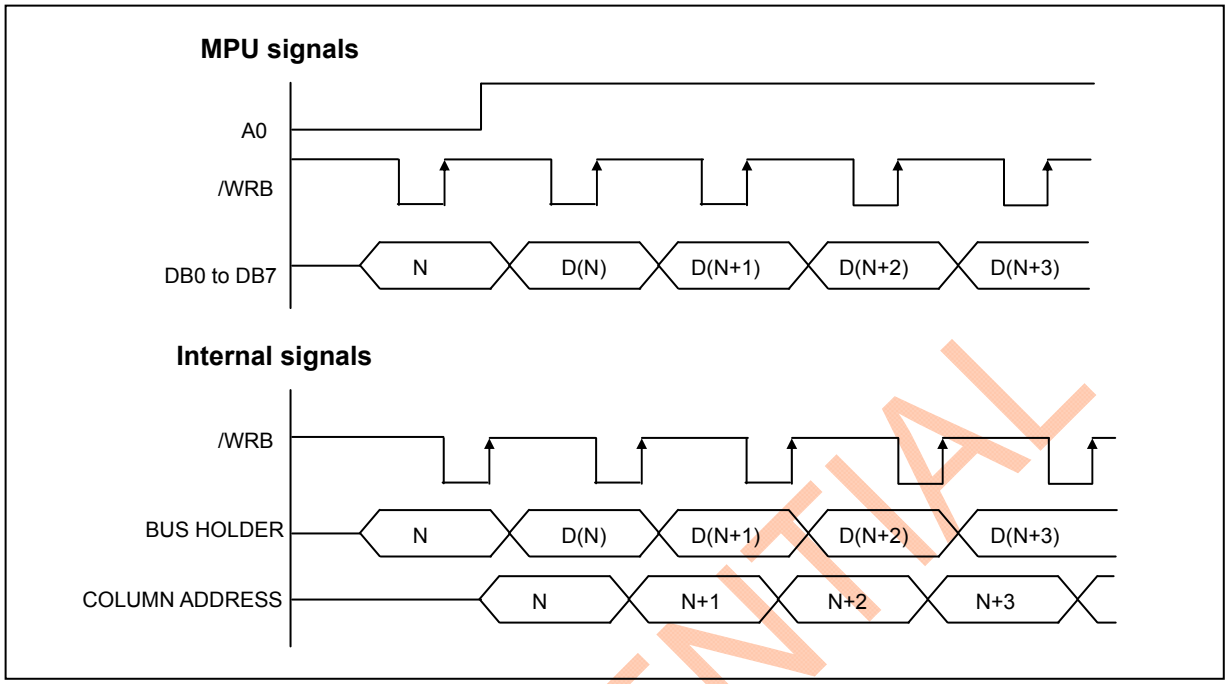
The Busy Flag indicates whether the IST7920 is still during operation or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the write cycle time is correct, the microprocessor needs not to check this flag before each instruction to improve the operation efficiency.

Data Transfer

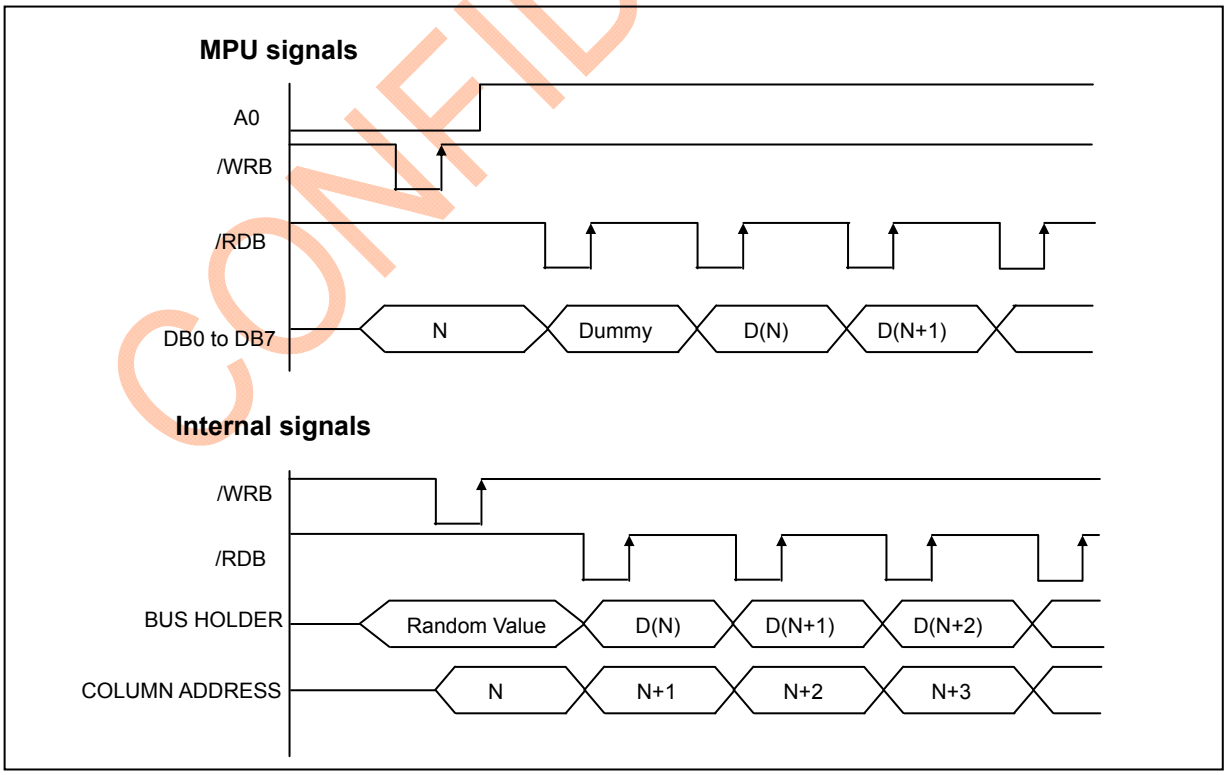
The IST7920 has a I/O bus holder stage to temporary storage the data received from MPU or on-chip RAM data requesting from MPU to read.

When user wants to read out the on-chip RAM data, after setting the address, a “dummy read” cycle must be inserted first to clean out the data stored in the output bus holder, so please just skip this dummy read data and the target RAM data can be read out from the second read cycle.

Write Timing



Read Timing



Display RAM Address Mapping

The IST7920 embedded a one-on-one bit-pixel mapping display RAM to storage the display image data. The RAM size is 128(row) x 128(column) bits. Each pixel can be selected when the row and column addresses are specified. Data is read from or written to by 8-bit width through DB0 to DB7. The display data & LCD display mapping is illustrated as below.

The display RAM is designed with two ports, so when display is turned on, the internal LCD display operation and MPU display RAM access is independent and will not affect each other.

Mono display mode SRAM mapping

ADC=0	AX		00H	01H	02H	03H	04H	05H	06H	07H	…	78H	79H	7AH	7BH	7CH	7DH	7EH	7FH
SHL=0	**SHL=1**	**AY**	Seg0	Seg1	Seg2	Seg3	Seg4	Seg5	Seg6	Seg7	…	Seg120	Seg121	Seg122	Seg123	Seg124	Seg125	Seg126	Seg127
COM0	COM127	00H	D0	D0	D0	D0	D0	D0	D0	D0		D0	D0	D0	D0	D0	D0	D0	D0
COM1	COM126	00H	D1	D1	D1	D1	D1	D1	D1	D1		D1	D1	D1	D1	D1	D1	D1	D1
COM2	COM125	00H	D2	D2	D2	D2	D2	D2	D2	D2		D2	D2	D2	D2	D2	D2	D2	D2
COM3	COM124	00H	D3	D3	D3	D3	D3	D3	D3	D3		D3	D3	D3	D3	D3	D3	D3	D3
COM4	COM123	00H	D4	D4	D4	D4	D4	D4	D4	D4		D4	D4	D4	D4	D4	D4	D4	D4
COM5	COM122	00H	D5	D5	D5	D5	D5	D5	D5	D5		D5	D5	D5	D5	D5	D5	D5	D5
COM6	COM121	00H	D6	D6	D6	D6	D6	D6	D6	D6		D6	D6	D6	D6	D6	D6	D6	D6
COM7	COM120	00H	D7	D7	D7	D7	D7	D7	D7	D7		D7	D7	D7	D7	D7	D7	D7	D7
…	…	…																	
COM120	COM7	0FH	D0	D0	D0	D0	D0	D0	D0	D0		D0	D0	D0	D0	D0	D0	D0	D0
COM121	COM6	0FH	D1	D1	D1	D1	D1	D1	D1	D1		D1	D1	D1	D1	D1	D1	D1	D1
COM122	COM5	0FH	D2	D2	D2	D2	D2	D2	D2	D2		D2	D2	D2	D2	D2	D2	D2	D2
COM123	COM4	0FH	D3	D3	D3	D3	D3	D3	D3	D3		D3	D3	D3	D3	D3	D3	D3	D3
COM124	COM3	0FH	D4	D4	D4	D4	D4	D4	D4	D4		D4	D4	D4	D4	D4	D4	D4	D4
COM125	COM2	0FH	D5	D5	D5	D5	D5	D5	D5	D5		D5	D5	D5	D5	D5	D5	D5	D5
COM126	COM1	0FH	D6	D6	D6	D6	D6	D6	D6	D6		D6	D6	D6	D6	D6	D6	D6	D6
COM127	COM0	0FH	D7	D7	D7	D7	D7	D7	D7	D7		D7	D7	D7	D7	D7	D7	D7	D7
SHL=0	**SHL=1**	**AY**	Seg127	Seg126	Seg125	Seg124	Seg123	Seg122	Seg121	Seg120	:	Seg7	Seg6	Seg5	Seg4	Seg3	Seg2	Seg1	Seg0
ADC=1	AX		00H	01H	02H	03H	04H	05H	06H	07H	…	78H	79H	7AH	7BH	7CH	7DH	7EH	7FH

Reset Initialization

The IST7920 provides both hardware (H/W) reset and software (S/W) reset function. When the RESB is setting to “L”, the H/W reset will be activated, or user can use S/W reset instruction to initialize the internal registers’ configurations, but the H/W reset and S/W reset covered range is different, please check the table listed as below.

The default H/W reset initializing settings are listed as below:

No.	Register	Description
1.	DON=0	Display OFF
2.	REV=0	Reverse display OFF
3.	ADC=0	SEG output direction SEG0 → SEG127
4.	SHL=0	COM output direction COM0 → COM127
5.	(internal status)	Serial interface internal register data clear
6.	BS=0	LCD bias
7.	EON=0	Entire display OFF
8.	AY=0	Row address
9.	AX=0	Column address
10.	(internal status)	SEG/COM output GROUND level
11.	ST=0	Display start line address = 0
12.	RR=10000000	Electronic volume register

★ For S/W reset , only the 1 ~ 11 items above will be reinitialized.

When doing the H/W reset (RESB = “L”), the PVC will also discharge to GROUND level internally, so when using external LCD power sources, please input these power sources only when the H/W reset process has been finished (RESB is backing to “H”) .

Command Table

*: Don't care

NO.	INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1	Set AX(2B)	0	0	1	1	0	0	0	0	0	0	Set AX
		0	0	AX7	AX6	AX5	AX4	AX3	AX2	AX1	AX0	Set col address
2	Power control(2B)	0	0	0	0	1	1	0	0	1	1	Power control
		0	0	*	*	VD1	VD0	VS	VC	VF1	VF0	
3	Bias select(2B)	0	0	0	0	1	1	0	0	0	0	Set LCD bias
		0	0	0	0	BS5	BS4	BS3	BS2	BS1	BS0	
4	Voltage generator clock frequency select(2B)	0	0	0	0	1	1	0	0	0	1	Three generators clock frequency divider select.
		0	0	0	0	VCK_SEL5	VCK_SEL4	VCK_SEL3	VCK_SEL2	VCK_SEL1	VCK_SEL0	
5	Temperature compensation select(2B)	0	0	0	0	1	1	0	0	1	0	Temperature compensation select
		0	0	0	0	0	0	0	TC2	TC1	TC0	
6	Sleep mode	0	0	0	0	1	1	1	0	0	SLP	Power save mode 1:sleep
7	OSC off	0	0	0	0	1	1	1	0	1	OSCOFF	0: OSC ON ; 1:OSC OFF
8	Display On/Off	0	0	0	0	1	1	1	1	0	DON	Turn on/off LCD. 0:OFF;1:ON
9	Set starting line(2B)	0	0	0	1	0	0	0	0	0	0	Set starting line
		0	0	0	ST6	ST5	ST4	ST3	ST2	ST1	ST0	Set starting line -LSB
10	Display control	0	0	0	1	1	0	SHL	ADC	EON	REV	Driver display control
11	Set windows AY(3B)	0	0	0	1	1	1	0	1	0	0	Set windows AY
		0	0	*	*	*	AYS4	AYS3	AYS2	AYS1	AYS0	AY start address
		0	0	*	*	*	AYE4	AYE3	AYE2	AYE1	AYE0	AY end address
12	Set windows AX(3B)	0	0	0	1	1	1	0	1	0	1	Set windows AX
		0	0	AXS7	AXS6	AXS5	AXS4	AXS3	AXS2	AXS1	AXS0	AX start address
		0	0	AXE7	AXE6	AXE5	AXE4	AXE3	AXE2	AXE1	AXE0	AX end address
13	S/W reset	0	0	0	1	1	1	0	1	1	0	Soft reset
14	spi3&spi4 read ram	0	0	0	1	1	1	0	1	1	1	SPI read ram data
15	spi3&spi4 read status	0	0	0	1	1	1	1	0	0	0	spi3&spi4&iic read status
16	Set Duty (2B)	0	0	1	0	0	1	0	0	0	0	Set Duty
		0	0	0	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	
17	Reference voltage select (2B)	0	0	1	0	1	1	0	0	0	1	Set Reference voltage mode
				RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0	
18	Frame Control (3B)	0	0	1	0	1	1	0	0	1	0	Set Frame Control
				LN7	LN6	LN5	LN4	LN3	LN2	LN1	LN0	
				LN15	LN14	LN13	LN12	LN11	LN10	LN9	LN8	
19	Set AY(2B)	0	0	0	0	0	0	0	0	0	1	Set AY address
		0	0	*	*	*	AY4	AY3	AY2	AY1	AY0	
20	Set booster	0	0	1	1	1	1	1	1	BT1	BT0	Set booster
21	Read Status	0	1	BUSY	ADC	DONB	RESB	0	0	0	0	Read the internal status
22	Write display data	1	0	Write data								Write data into Display RAM
23	Read display data	1	1	Read data								Read data from Display RAM
24	Temperature sensor ON/OFF	0	0	1	1	1	0	0	0	0	TSON	TSON=1, enable; TSON=0, disable
25	Temperature sensor register	0	0	1	1	1	0	0	1	0	0	Read temperature sensor register
		0	1	1	TS6	TS5	TS4	TS3	TS2	TS1	TS0	

26	Temperature sensor measure times	0	0	1	1	1	0	0	1	0	1	Select the measure times
				*	TST2	TST1	TST0	*	TSMT2	TSMT1	TSMT0	
27	Temperature coefficient	0	0	1	1	1	0	0	1	1	0	Using for temperature sensor
				TCA3	TCA2	TCA1	TCA0	TCB3	TCB2	TCB1	TCB0	
		0	0	1	1	1	0	0	1	1	1	
				TCC3	TCC2	TCC1	TCC0	TCD3	TCD2	TCD1	TCD0	
		0	0	1	1	1	0	1	0	0	0	
				TCE3	TCE2	TCE1	TCE0	TCF3	TCF2	TCF1	TCF0	
		0	0	1	1	1	0	1	0	0	1	
				TCG3	TCG2	TCG1	TCG0	TCH3	TCH2	TCH1	TCH0	
28	NOP	0	0	1	1	1	0	0	0	1	1	Dummy command
29	Efuse mode	0	0	1	0	0	0	0	0	0	0	Efuse burning mode
30	PVC adjust(2B)	0	0	0	0	1	0	0	1	0	0	PVC adjusting
		0	0	0	0	0	0	PVC_ADJ3	PVC_ADJ2	PVC_ADJ1	PVC_ADJ0	
31	PVC_ADJ fuse enable	0	0	0	0	0	0	1	0	0	PVC_enable	PVC_ADJ fuse enable
32	Efuse program enable	0	0	1	1	1	1	0	1	0	0	Efuse program enable
33	Efuse program start	0	0	0	0	1	0	0	0	0	0	Efuse program start
34	IST command entry	0	0	1	0	0	0	1	0	0	0	IST command entry
35	Exit entry	0	0	1	1	1	0	0	0	1	1	Exit to normal command access

COMMAND DESCRIPTION

1. Set AX (Column) Address

Set the AX address of display data RAM for MPU Write/Read access. After setting the AY (row) and/or AX (column) address, user can write/read the internal display RAM consecutively. When the AX (Row) address auto-incremented at the end, the AY address will auto-incremented by +1.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	0	0
0	0	AX7	AX6	AX5	AX4	AX3	AX2	AX1	AX0

2. Power Control

Internal Power supply circuits control. For details please refer to the “Power Supply Circuits” section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0	1	1
0	0	*	*	VD1	VD0	VS	VC	VF1	VF0

VD [1:0]: VDDL voltage generator select:

VDLS	VD[1:0]	Description
1	00B	External power connect to VDDL
0	00B	VDD1
*	01B	1.8V regulator (**first VS=1 VDLS=0, delay more than 10ms then VDLS=1**)
0	10B	1/2 VDD1
0	11B	2/3 VDD1

Note: when VDLS is H, must keep VD [1-0] all “L” to avoid current Leakage.

VS=”0”/”1” Internal voltage reference circuit OFF/ON;

VC=”0”/”1” PVC voltage generator OFF/ON;

VF [1:0]: Driver voltage generator operation mode select:

VF[1:0]	Description
00B	Shut off the driver voltage generator.
01B	Switch capacitor mode.
10B	Switch capacitor and voltage follower mode.
11B	Voltage follower mode.

3. Bias select

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0	0	0
0	0	0	0	BS5	BS4	BS3	BS2	BS1	BS0

BS[5:0]	111111	111110	111101	·····	000011	000010	000001	000000

BIAS	1/15.875	1/15.750	1/15.625	……	1/8.375	1/8.250	1/8.125	1/8

4. Voltage Generator Clock Frequency select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0	0	1
0	0	0	0	VCK_SEL5	VCK_SEL4	VCK_SEL3	VCK_SEL2	VCK_SEL1	VCK_SEL0

Control bits [DB5:DB4] are for F_{PVC}, [DB3:DB2] are for F_{VDL} and [DB1:DB0] are for F_{DRIVER}

[H:L] = [DB5:DB4] / [DB3:DB2] / [DB1:DB0]					$F_{PVC}=F_{OSC}*F\_DIV[5:4]*2$
VCK_SEL[H:L]	11	10	01	00	$F_{VDL}= F_{OSC}*F\_DIV[5:4]*F\_DIV[3:2] *2$
F_DIV[H:L]	1/1	1/4	1/16	1/64	$F_{DRIVER}= F_{OSC}*F\_DIV[5:4]*F\_DIV[1:0] *2$

5. Temperature Compensation Select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	0	0	TC2	TC1	TC0

Set PVC temperature compensation coefficient (%-per-degree-C)

TC[2:0]	000	001	010	011	100	101	110	111
% per ℃	-0.00	-0.02	-0.04	-0.06	-0.08	-0.10	-0.12	-0.14

6. Sleep Mode

Sleep mode only happen at SLP=1, It'll stop all the operations in this chip, as long as there are no accesses from the MPU, the power consumption is close to the static leakage current. Set SLP=0 to exit sleep mode. The internal status during sleep mode is as below:

The oscillator circuit and the LCD power supply circuit are turned off.

All liquid crystal drive circuits are stop, all the LCD driving outputs (SEGx/COMx) output GROUND level.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	SLP

7. OSC OFF

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	OSCOFF

The oscillator circuit will be turned off when OSCOFF set "H".

8. Display ON / OFF

LCD display ON / OFF select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	DON

DON=1 Display ON; DON=0 Display OFF.

9. Display Starting Line

Set the starting line address for the first common output.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	0	0
0	0	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0

ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
…	…	…	…	…	…	…	…	…
0	1	1	1	1	1	1	1	127

10. Display control

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	SHL	ADC	EON	REV

SHL: Select (Common Output Mode Select)

SHL = 0: COM0 → COM (N-1)
SHL = 1: COM (N-1) → COM0
N defines as duty setting, reference as “SET DUTY”.

ADC:

Defines the relationship between RAM column address and segment driver. The detailed mapping please referred to the “Display RAM Address Mapping” chapter.
ADC = 0: SEG0 → SEG127
ADC = 1: SEG127 → SEG0

EON:

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. This instruction will not change the original display RAM data and has higher priority than the reverse display ON / OFF instruction.

EON = 0: Normal display
EON = 1: Entire display ON

REV:

Reverse the lit and unlit display relation between RAM bit data and LCD cell. This setting will not change the original display RAM data.

REV	RAM bit data = “1”	RAM bit data = “0”
0	LCD pixel will accumulated ON voltage	LCD pixel will accumulated OFF voltage
1	LCD pixel will accumulated OFF voltage	LCD pixel will accumulated ON voltage

11. Set windows AY

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	0	0
0	0	*	*	*	AYS4	AYS3	AYS2	AYS1	AYS0
0	0	*	*	*	AYE4	AYE3	AYE2	AYE1	AYE0

AYS4-0: Define start page address of display windows; AYE4-0: Define end page address of display windows.

12. Set windows AX

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	0	1
0	0	AXS7	AXS6	AXS5	AXS4	AXS3	AXS2	AXS1	AXS0
0	0	AXE7	AXE6	AXE5	AXE4	AXE3	AXE2	AXE1	AXE0

AXS7-0: Define start column address of display windows; AXE9-0: Define end column address of display windows.

13. S/W Reset

This instruction will activate the internal S/W reset operation. The covered ranged is different with H/W reset, for details please refer to the “Reset Initialization” section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	1	0

14. SPI3&SPI4 read ram

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	1	1

15. SPI3&SPI4 read status

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	1	0	0	0

16. Set Duty

This instruction will activate the internal S/W reset operation. The covered ranged is different with H/W reset, for details please refer to the “Reset Initialization” section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	0
0	0	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0

DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	Duty Ratio
0	0	0	0	X	X	X	X	X
0	0	0	1	0	0	0	0	1/16
0	0	0	1	1	0	0	0	1/24
0	0	1	0	0	0	0	0	1/32
0	0	1	0	1	0	0	0	1/40

0	0	1	1	0	0	0	0	1/48
0	0	1	1	1	0	0	0	1/56
0	1	0	0	0	0	0	0	1/64
0	1	0	0	1	0	0	0	1/72
0	1	0	1	0	0	0	0	1/80
0	1	0	1	1	0	0	0	1/88
0	1	1	0	0	0	0	0	1/96
0	1	1	0	1	0	0	0	1/104
0	1	1	1	0	0	0	0	1/112
0	1	1	1	1	0	0	0	1/120
1	0	0	0	0	0	0	0	1/128

After setting DUTY, COM0~COM (N-1) is select, N=DUTY [7:0], 1/8 per step.

17. Reference Voltage Select (double byte command)

The Reference voltage select instruction consists of 2-byte command. The 1st instruction sets reference voltage mode and the 2nd one is the contents of reference voltage register. These two instructions must be executed adjacently or the following commands sequence will be misinterpreted and lead to unexpected results.

The 1st instruction: Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	0	0	1

The 2nd instruction: Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0

RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0	Reference voltage Parameter (α)	PVC	Contrast
0	0	0	0	0	0	0	0	0（default）	Minimum	Low
0	0	0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	128	:	:
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	254		
1	1	1	1	1	1	1	1	255	Maximum	High

PVC Voltage Calculation:

$$PVC(V) = \underbrace{4.000}_{A} + \underbrace{37.209 * [RR(\alpha) + PVC\_ADJ]/1000}_{B}$$

Note: when fuse is not burning, PVC_ADJ = 0

18. Frame Control (Three bytes command)

The Frame Control instruction consists by three commands. The 1st instruction sets Frame Control mode, the 2nd and 3rd command set the Frame frequency DIV number.

The 1st instruction: sets Frame Control mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	0	1	0

The 2nd and 3rd instruction:

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	LN7	LN6	LN5	LN4	LN3	LN2	LN1	LN0
0	0	LN15	LN14	LN13	LN12	LN11	LN10	LN9	LN8

LN15~0: DIV number by inside oscillator (TBD)

Row frequency = F_{OSC}/ (LN15~0+1) Frame frequency = Row frequency / DUTY7~0 (at 25℃)

19. Set AY Address

Sets the page Address of display data RAM for MPU Write/Read access. After setting the row and/or Column address, user can write/read the internal display RAM consecutively. The Column address will auto-incremented by +1.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1
0	0	*	*	*	AY4	AY3	AY2	AY1	AY0

20. Set Booster

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	BT1	BT0

BT1-0: Define the DCDC booster operation mode; select the suitable BT1-0 will save the power consumption.

BT<1:0>	00	01	10	11
PVC_{MAX}	2*VDD2-0.3	3*VDD2-0.3	4*VDD2-0.3	5*VDD2-0.3

Note: make sure the condition below to make Power operates efficiency.

1. PVC< **PVC_{MAX}**
2. PVC > **PVC_{MAX} –VDD**

21. Read Status

Indicate the internal status of the IST7920. When use SPI3, SPI4 or IIC interface, it must send the command 78H before read operation.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	1	0	0	0
0	1	BUSY	ADC	ON/OFF	RESB	0	0	0	0

Only use in SPI3, SPI4 or IIC interface

Flag	Description
BUSY	BUSY = 1 : The chip is still under processing, including reset initialization BUSY = 0 : The chip is free to accept MPU commands
ADC	ADC = 1 : SEG direction is SEG127 → SEG0 ADC = 0 : SEG direction is SEG0 → SEG127
DISPLAY ON/OFF	ON/OFF = 1 : Display is turned off ON/OFF = 0 : Display is turned on * The polarity is reversed with DON command!
RESET	RESET = 0 : The chip is doing the H/W or S/W reset RESET = 1 : The chip is not doing the reset operation

22. Write Display Data

8-bit display data can be written to the display RAM location specified by the column address and row address by this instruction. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed rows.

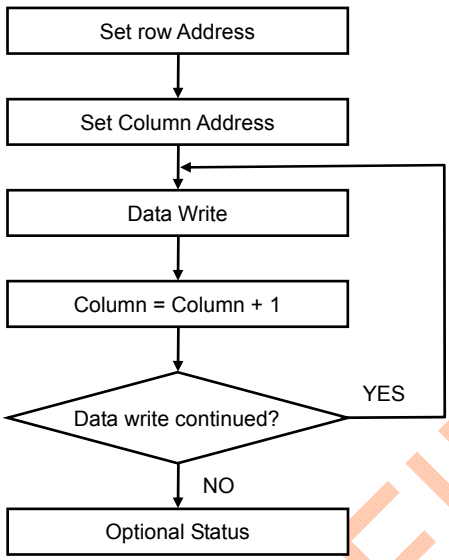
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

23. Data Read Display Data

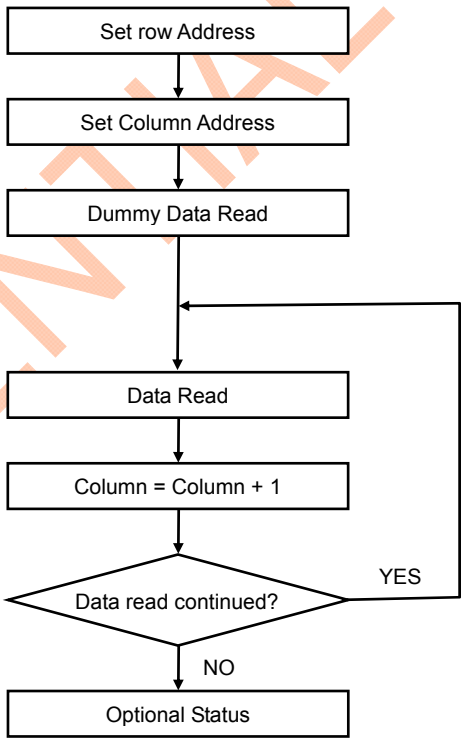
8-bit display data RAM specified by the column address and row address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously can continuously read data from the addressed row. A dummy read is required after specified the target column and/or row address.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Display RAM Write Sequence



Display RAM Read Sequence



24. Temperature sensor ON/OFF

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	TSON

TSON: The instruction determines the temperature sensor which is ON/OFF. When TSON=1, the temperature sensor turns on. When TSON=0, it turns off.

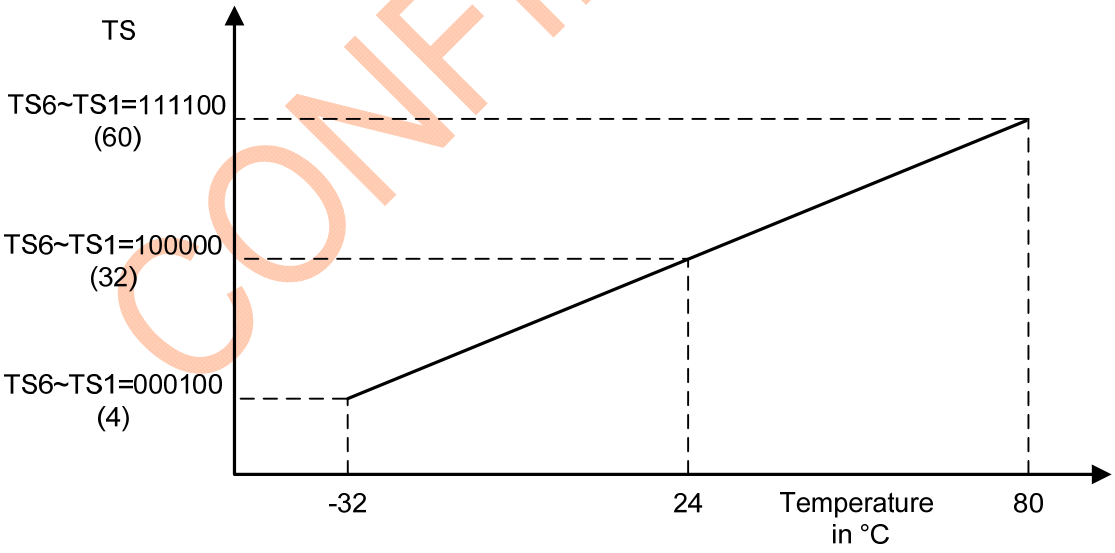
Note: TSON=0 only stop the temp. sensing, the sensor output will also stop refreshing and the readout will keep at the data last sampled, but the contrast corrections is still under operation.

To effectively turn off temp. compensation one must load all the temp. Coefficient table with all zeros(P43 "**Temperature Coefficient"**).

25. Temperature Sensor (Read sensor register)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0
0	1	1	TS6	TS5	TS4	TS3	TS2	TS1	TS0

The instruction has double byte. When use it, send the command E4H first and then send read signal.



6 bit output, resolution 2℃/code, we can get Temperature reading from the following formula.

TS = (Temperature+40)/2

Temperature = TS*2 – 40℃

26. Temperature Sensor Measure Times

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	1
		*	TST2	TST1	TST0	*	TSMT2	TSMT1	TSMT0

TSMT: It provide to select the times which the temperature sensor measure, and average the values.

TSMT2	TSMT1	TSMT0	Average times
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

TST: It provide to select the frequency which the temperature sensor measure.

TST2	TST1	TST0	Frequency (KHz)
0	0	0	$F_{OSC}/4$
0	0	1	$F_{OSC}/8$
0	1	0	$F_{OSC}/16$
0	1	1	$F_{OSC}/32$
1	0	0	$F_{OSC}/64$
1	0	1	$F_{OSC}/128$
1	1	0	$F_{OSC}/256$
1	1	1	$F_{OSC}/512$

27. Temperature Coefficient

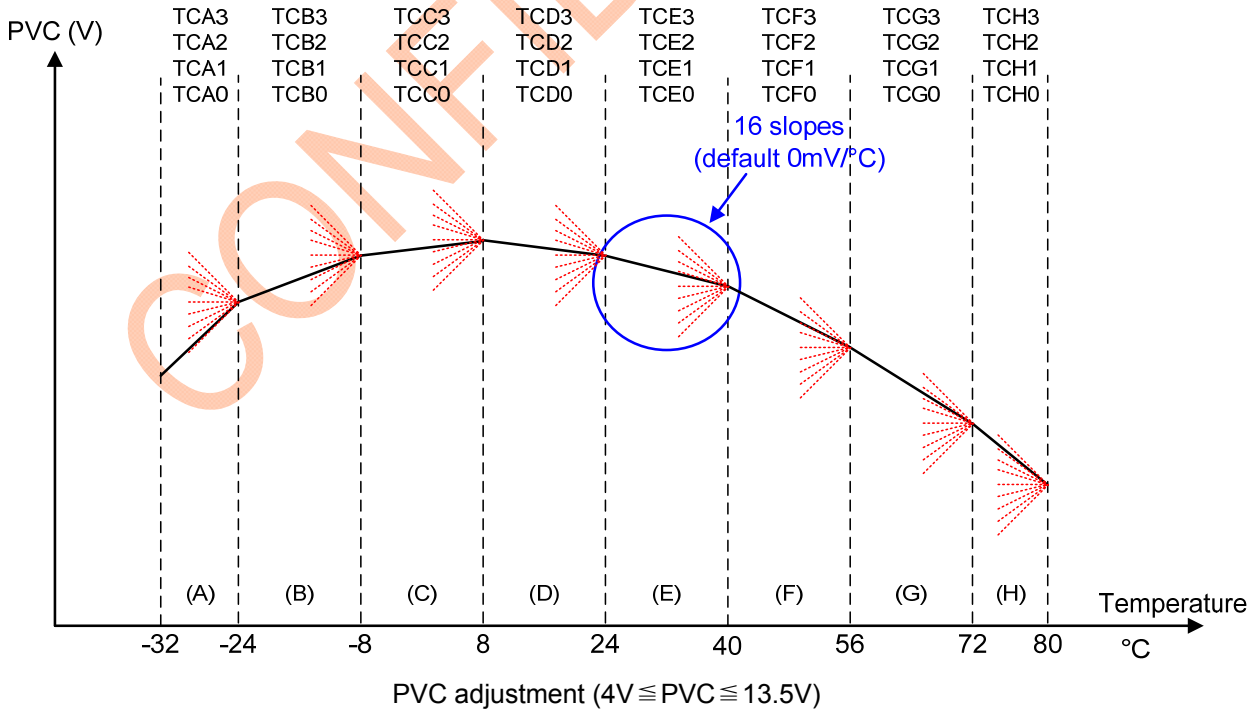
ID	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	0	0	1	1	1	0	0	1	1	0
			TCA3	TCA2	TCA1	TCA0	TCB3	TCB2	TCB1	TCB0
	0	0	1	1	1	0	0	1	1	1
			TCC3	TCC2	TCC1	TCC0	TCD3	TCD2	TCD1	TCD0
	0	0	1	1	1	0	1	0	0	0
			TCE3	TCE2	TCE1	TCE0	TCF3	TCF2	TCF1	TCF0
	0	0	1	1	1	0	1	0	0	1
			TCG3	TCG2	TCG1	TCG0	TCH3	TCH2	TCH1	TCH0

PVC Compensation

TCX3/TCX2/TCX1/TCX0: Set the temperature compensation slope, there are 16 slopes, it is ranged from -80mV/℃ to +70mV/℃. There are 8 regions A/B/C/D/E/F/G/H can be set separately. Customer can select one slope of temperature compensation coefficient for each temperature region. Each temperature region is 16°C.

Note：TCX3 is represented as TCA3 or TCB3 or TCC3 or TCD3 or TCE3 or TCF3 or TCG3 or TCH3.
TCX2 is represented as TCA2 or TCB2 or TCC2 or TCD2 or TCE2 or TCF2 or TCG2 or TCH2.
TCX1 is represented as TCA1 or TCB1 or TCC1 or TCD1 or TCE1 or TCF1 or TCG1 or TCH1.
TCX0 is represented as TCA0 or TCB0 or TCC0 or TCD0 or TCE0 or TCF0 or TCG0 or TCH0.

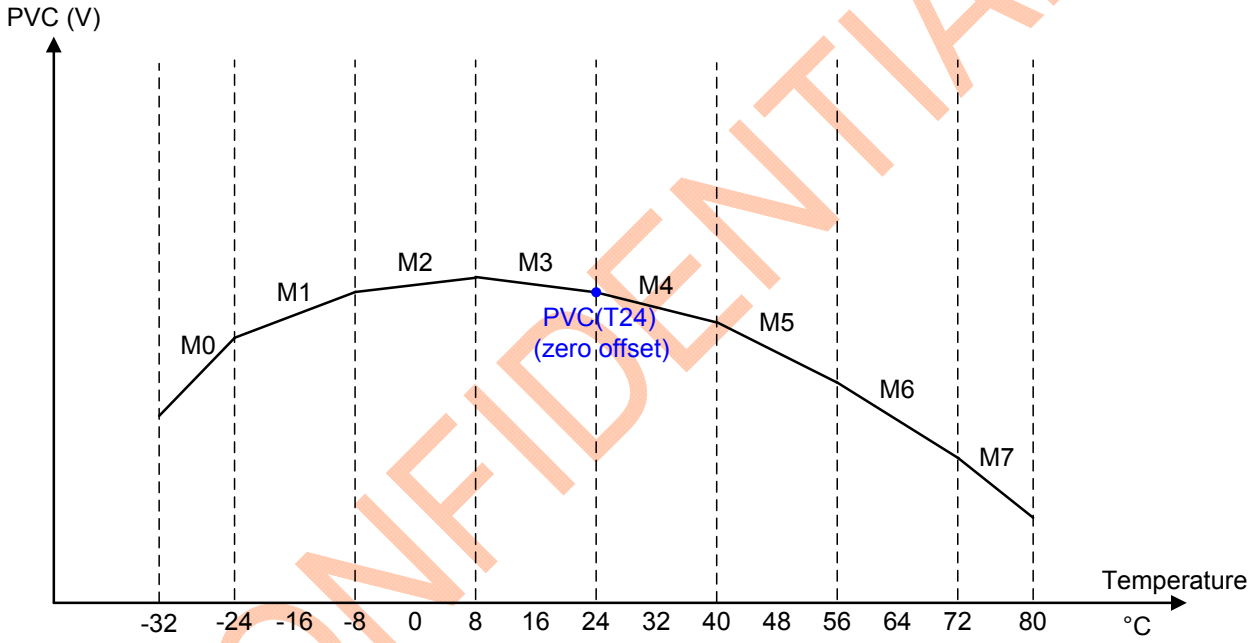
TCX3	TCX2	TCX1	TCX0	SLOPE(Mx)
1	0	0	0	-20 mV/℃
1	0	0	1	-17.5 mV/℃
1	0	1	0	-15 mV/℃
1	0	1	1	-12.5 mV/℃
1	1	0	0	-10 mV/℃
1	1	0	1	-7.5 mV/℃
1	1	1	0	-5 mV/℃
1	1	1	1	-2.5 mV/℃
0	0	0	0	0 mV/℃
0	0	0	1	+2.5 mV/℃
0	0	1	0	+5 mV/℃
0	0	1	1	+7.5 mV/℃
0	1	0	0	+10 mV/℃
0	1	0	1	+12.5 mV/℃
0	1	1	0	+15 mV/℃
0	1	1	1	+17.5 mV/℃



Mx means temperature compensation slope, x=0, 1, 2, ……, 7. These 8 Mx each separately represent one temperature region from region A to H. The relations between Mx and PVC quantity due to temperature PVC(T) are

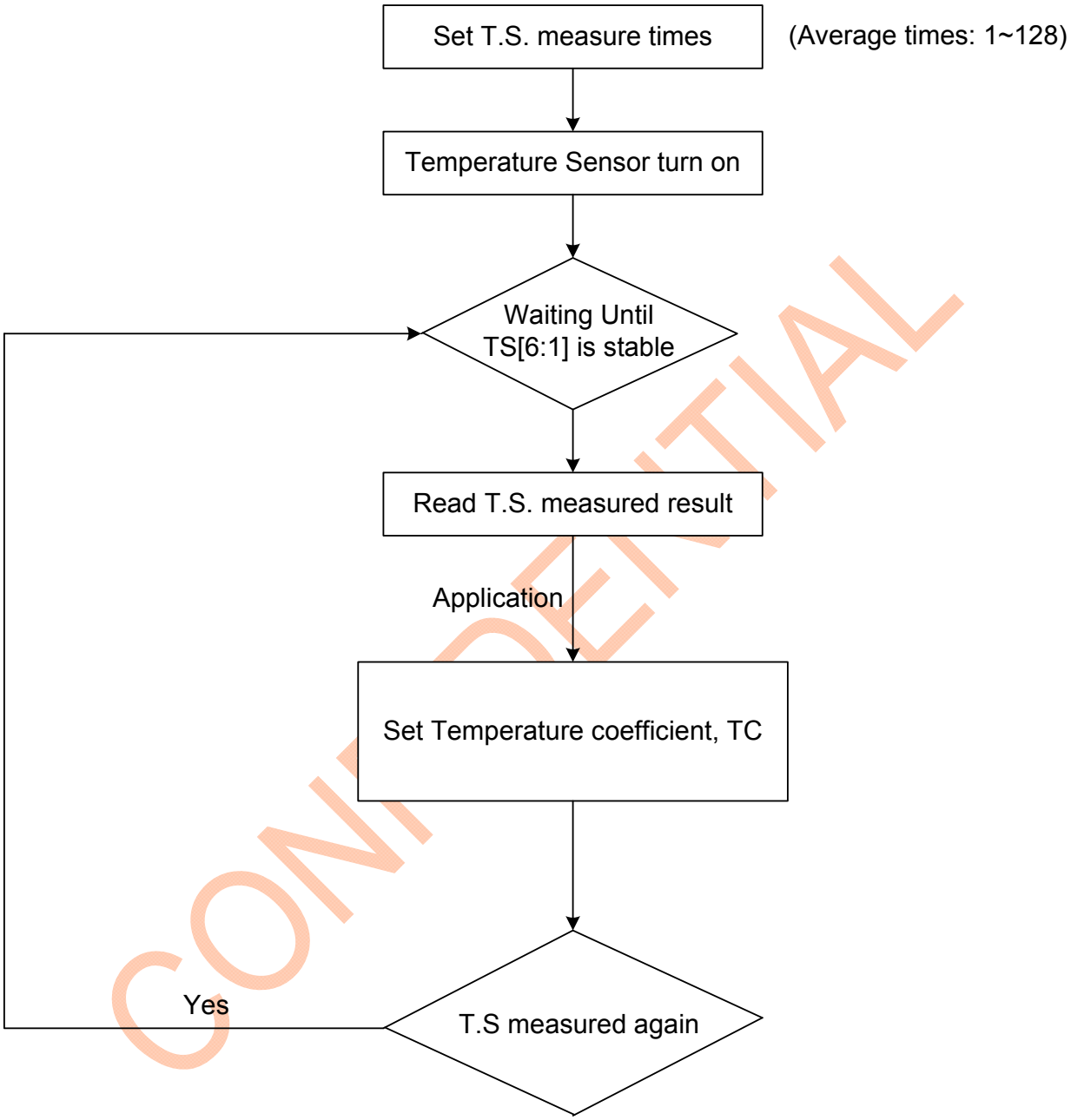
described in the equation shown in table as follows.

Temperature Range	Equation PVC(T) at temperature=T°C
-32°C ≦ T < -24°C	PVC(T) = PVC(T24) - (-24 - T) x M0 - (M1 + M2 + M3) x 16
-24°C ≦ T < -8°C	PVC(T) = PVC(T24) - (-8 - T) x M1 - (M2 + M3) x 16
-8°C ≦ T < 8°C	PVC(T) = PVC(T24) - (8 - T) x M2 - M3 x 16
8°C ≦ T < 24°C	PVC(T) = PVC(T24) - (24 - T) x M3
24°C ≦ T < 40°C	PVC(T) = PVC(T24) + (T - 24) x M4
40°C ≦ T < 56°C	PVC(T) = PVC(T24) + (T - 40) x M5 + M4 x 16
56°C ≦ T < 72°C	PVC(T) = PVC(T24) + (T - 56) x M6 + (M5 + M4) x 16
72°C ≦ T < 80°C	PVC(T) = PVC(T24) + (T - 72) x M7 + (M6 + M5 + M4) x 16



PVC can be adjusted at different temperatures to maintain optimal contrast. There are 8 temperature regions, A/B/C/D/E/F/G/H. For each temperature region, a different temperature coefficient can be selected. Each coefficient can be selected for a choice of 16 different slopes by setting TCA3~0, TCB3~0, TCC3~0, TCD3~0, TCE3~0, TCF3~0, TCG3~0, TCH3~0. Note that the controlled PVC will not be changed linearly, but in 10mV steps. Slopes TCA3~0, TCB3~0, TCC3~0, TCD3~0, TCE3~0, TCF3~0, TCG3~0, TCH3~0, are overridden by EEPROM values if these are set.

Temperature Sensor Application Flow



28. NOP

No-Operation command (dummy command).

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

29. Efuse mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0

30. PVC adjust (2B)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	1	0	0
0	0	0	0	0	0	PVC_ADJ3	PVC_ADJ2	PVC_ADJ1	PVC_ADJ0

Note:

(1) when adjusting, PVC_ADJ3-0 writing order is DB3, DB2, DB1, DB0;

(2) when burning, PVC_ADJ3-0 writing order is DB2,DB1,DB0,DB3.

PVC adjusting table

PVC_ADJ	PVC adjusting (step=37.209mV)
0x00	+0
0x01	+1step
0x02	+2step
0x03	+3step
0x04	+4step
0x05	+5step
0x06	+6step
0x07	+7step
0x08	-8step
0x09	-7step
0x0A	-6step
0x0B	-5step
0x0C	-4step
0x0D	-3step
0x0E	-2step
0x0F	-1step

Efuse burning flow

Step	A0	RW	Command	Description
0	--	--	3ch	■ Set Display off
1^{step1}	0	0	80h	■ Enter EFUSE command mode
1^{step2}	0	0	80h	■ Enter EFUSE command mode
1^{step3}	0	0	80h	■ Enter EFUSE command mode
1^{step4}	0	0	80h	■ Enter EFUSE command mode
2^{step1}	0	0	24h	■ Set command for adjusting PVC_ADJ
2^{step2}	0	0	0xh	■ PVC_ADJ3~0
3	0	0	WaitKey	■ Wait VFSOURCE supply, using 8V
4	0	0	09h	■ Enable PVC_ADJ fuse
5	0	0	F4h	■ EFUSE program enable
6	0	0	20h	■ EFUSE program start
7	0	0	(Waiting)	■ Waiting EFUSE burning, waiting 20mS
8	0	0	E3h	■ Use NOP command to release EFUSE command mode

31. PVC_ADJ fuse enable

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	0	0	PVC_ enable

Note: when PVC_enable = 1, enable fuse PVC_ADJ.

32. Efuse program enable

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	0

33. Efuse program start

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	0	0	0

34. IST command entry

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0

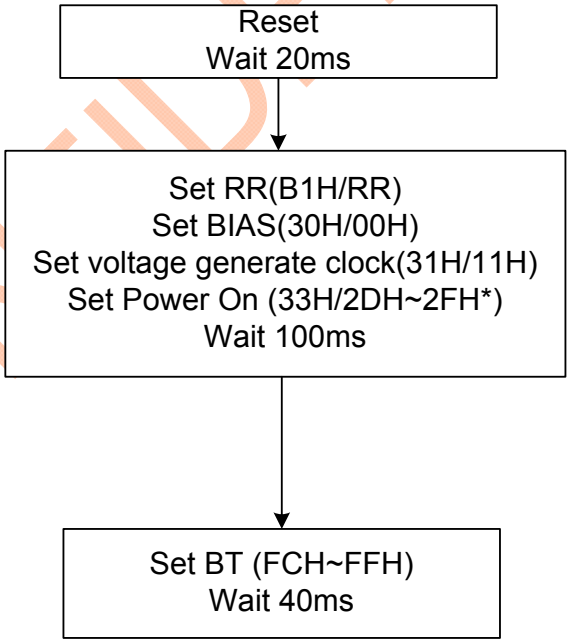
35. Exit entry

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

IST command write Flow

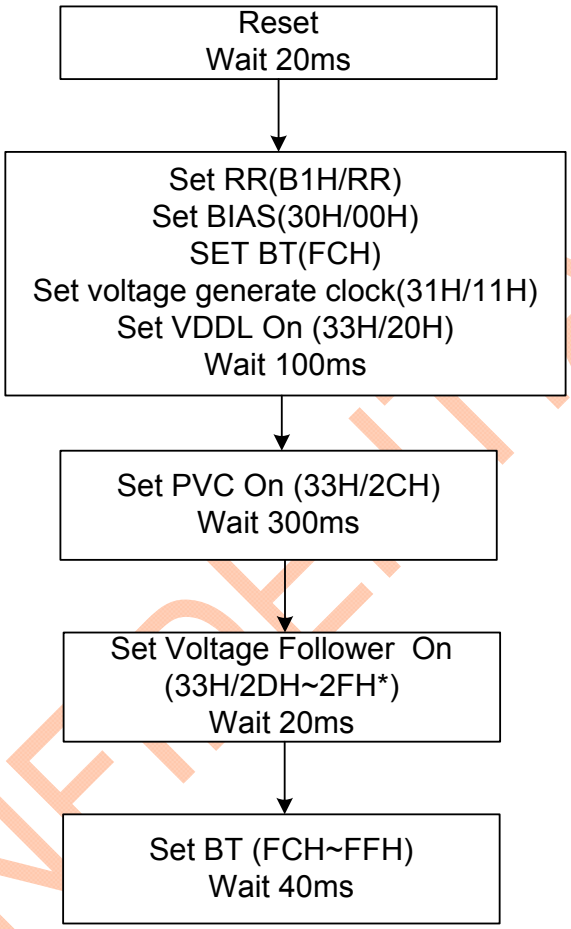
Step	A0	RW	Command	Description
1^{step1}	0	0	88h	■ Enter IST command mode
1^{step2}	0	0	88h	■ Enter IST command mode
1^{step3}	0	0	88h	■ Enter IST command mode
1^{step4}	0	0	88h	■ Enter IST command mode
2	0	0	Reserve	■ Reserve
3	0	0	E3h	■ Use NOP command to release IST command mode

Power on Sequence (VDDIO=VDD1/2/3>=2.4V, VDDL=1/2VDD or 2/3VDD)



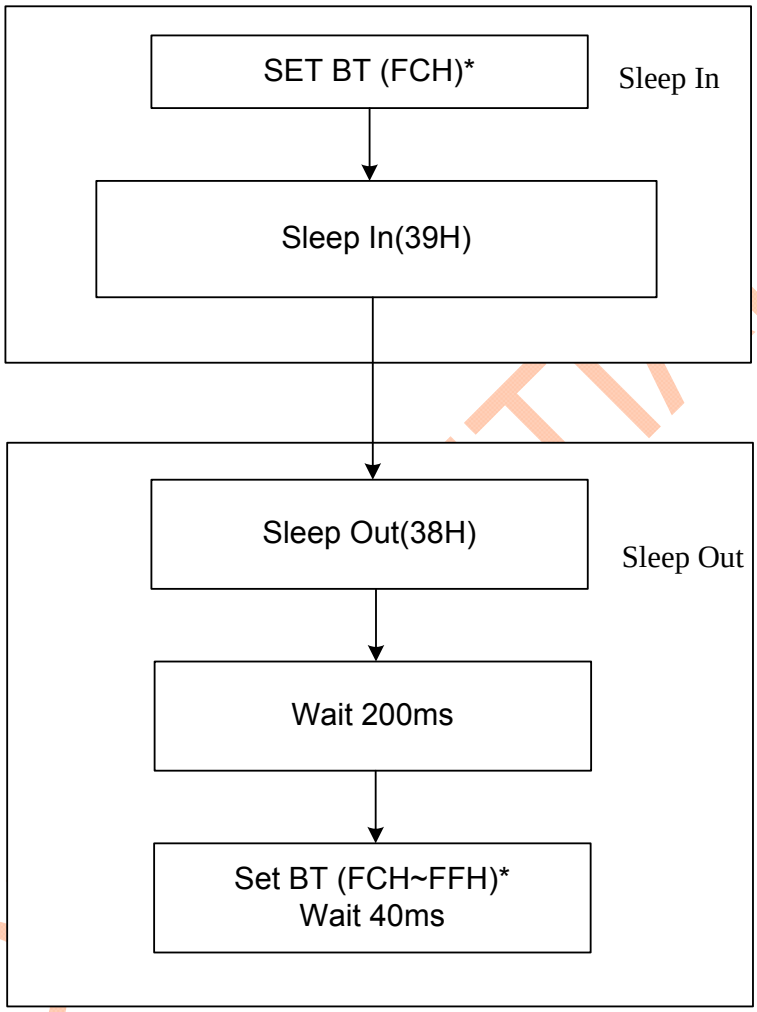
Note: 2DH can be 2EH and 2FH

Power on Sequence (VDDIO=VDDL=VDD1/2/3<=2.4V)



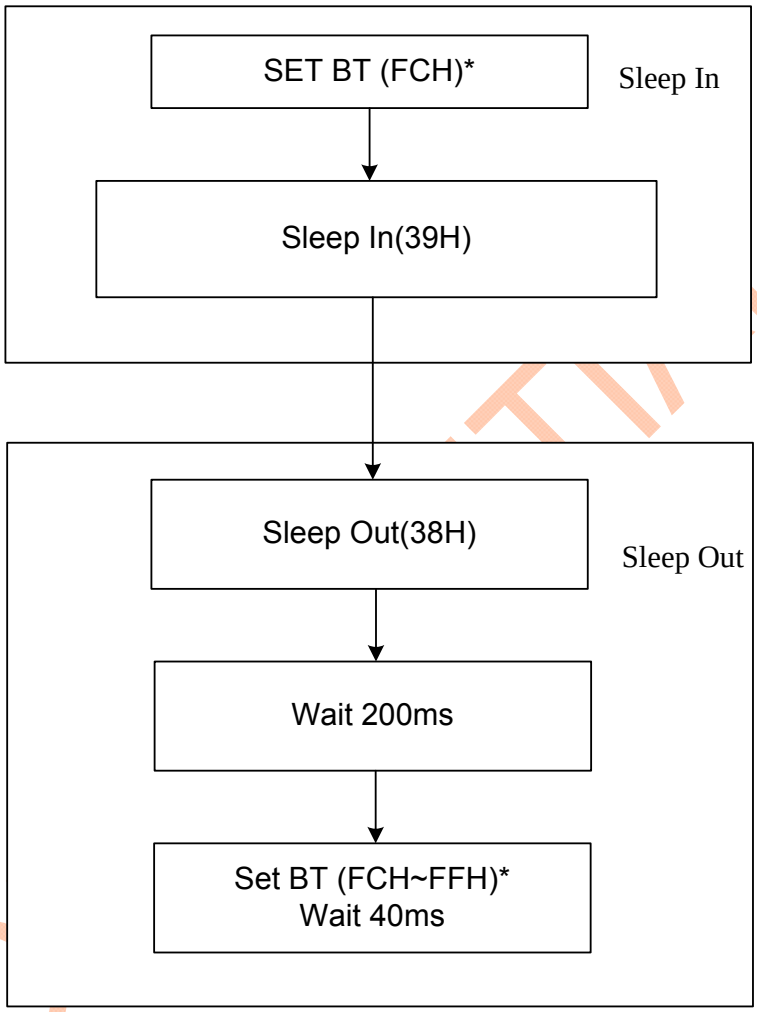
Note: 2DH can be 2EH and 2FH

Sleep Sequence (VDDIO =VDD1/2/3>2.4V, VDDL=1/2VDD or 2/3VDD)



Note: If select NxVDD(N>=4) booster, BT must set FCH(2xVDD) before Sleep In, and BT re-set the Booster again after Sleep Out

Sleep Sequence (VDDIO=VDDL=VDD1/2/3<=2.4V)



Note: If select NxVDD(N>=4) booster, BT must set FCH(2xVDD) before Sleep In, and BT re-set the Booster again after Sleep Out

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD1/VDD2/VDD3/VDDL/ VDDIO	-0.3 ~ 5	V
	PVCO/PVCI/PVCS	-0.3 ~ 15	V
Input voltage range	V_{IN}	-0.3 to VDD1 + 0.3	V
Operating temperature range	T_{OPR}	-40 to +90	℃
Storage temperature range (Bare chip)	T_{STR}	-55 to +125	℃

NOTES:

1. All voltages are based on VSS1=VSS2=VSS3=0V;

2. If supply voltage exceeds the absolute maximum range, this LSI may be damaged permanently.

DC CHARACTERISTICS

Ta=−30°C to +80 °C, unless otherwise specified.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage(1)		VDDL VDDIO		1.5	-	3.6	V	VDDL VDDIO *1
Operating Voltage(2)		VDD1~3		1.8	-	3.6	V	VDD1~3 *1
Operating Voltage(3)		PVCO PVCI PVCS		-	-	External =13.5 Internal =13.5	V	PVCO PVCI PVCS
EFUSE power		VFSOURCE		6.5	-	7	V	VFSOURCE
Input voltage	High	V_{IH}		0.8*VDDIO	-	VDDIO	V	*2
	Low	V_{IL}		VSS1	-	0.2*VDDIO		
Output voltage	High	V_{OH}	VDDIO = 3.3V, I_{OUT} = 1mA	0.8*VDDIO	-	VDDIO	V	*3
	Low	V_{OL}	VDDIO = 3.3V, I_{OUT} = 1mA	VSS1	-	0.2*VDDIO		
Input leakage current		I_{IL}	V_{IN} = VDDIO or VSS1	-1.0	-	+1.0	μA	*2
LCD driver ON Resistance		R_{ON}	Ta=25℃, PVC= 7.5V	-	2.5	-	kΩ	COMx *4
				-	2.5	-	kΩ	SEGx *4
Oscillator frequency (internal)		F_{OSC}	VDD1=3.3V, Ta = 25℃	115	128	141	KHz	
Frame Frequency		FR	Duty=1/128, PVC=7.0V, Ta=25℃	45	50	55	Hz	

Current consumption: During Display, with internal power system (bare die).

Test Pattern	Symbol	Condition	Rating			Unit	Pin used
			Min.	Typ.	Max.		
Display Pattern: SNOW	I_{VDD}	VDD1~3=3.3V, PVC=6V Power control=2D(HEX) Bias=1/8, frame rate=35Hz Booster=FC(2X), Ta=25℃	-	20	-	μA	I_{VDD1} + I_{VDD2} + I_{VDD3} + *5
Sleep Mode	I_{VDD}	VDD1~3=3.3V, PVC=6V Power control=2D(HEX) Bias=1/8, Booster=FC(2X), Ta=25℃	-	-	1	μA	

NOTE

*1. Although the wide range of DC operating voltages is guaranteed, but if the voltage fluctuation is too large during MPU accessing, the performance can't be guaranteed;

*2. CS1B, CS2, RESB, A0, RW_WRB, E_RDB, DB [7:0], C68, PS, IIC, CLS, CL, pins.

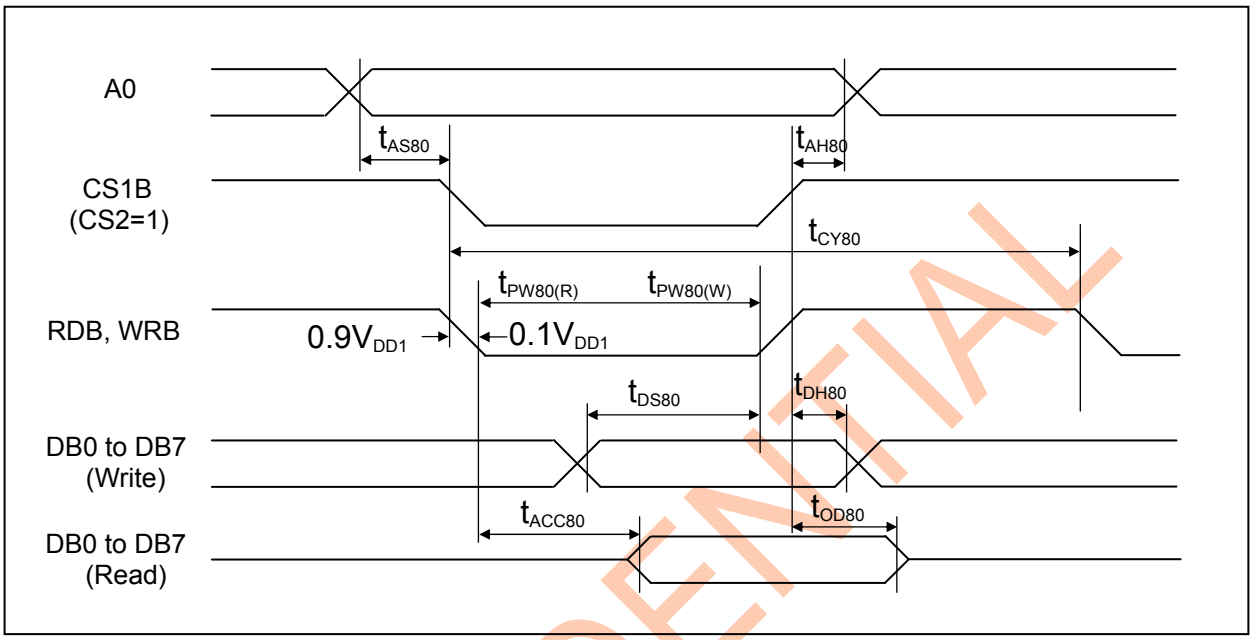
*3. DB [7:0];

*4. Resistance value when 0.1mA is applied during the ON status of the output pin SEGx or COMx.
RON= ΔV / 0.1 [KΩ] (ΔV: voltage change when 0.1mA is applied in the ON status.)

*5. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU & the LCD outputs (COMx, SEGx) are just floating, without any loading

AC CHARACTERISTICS

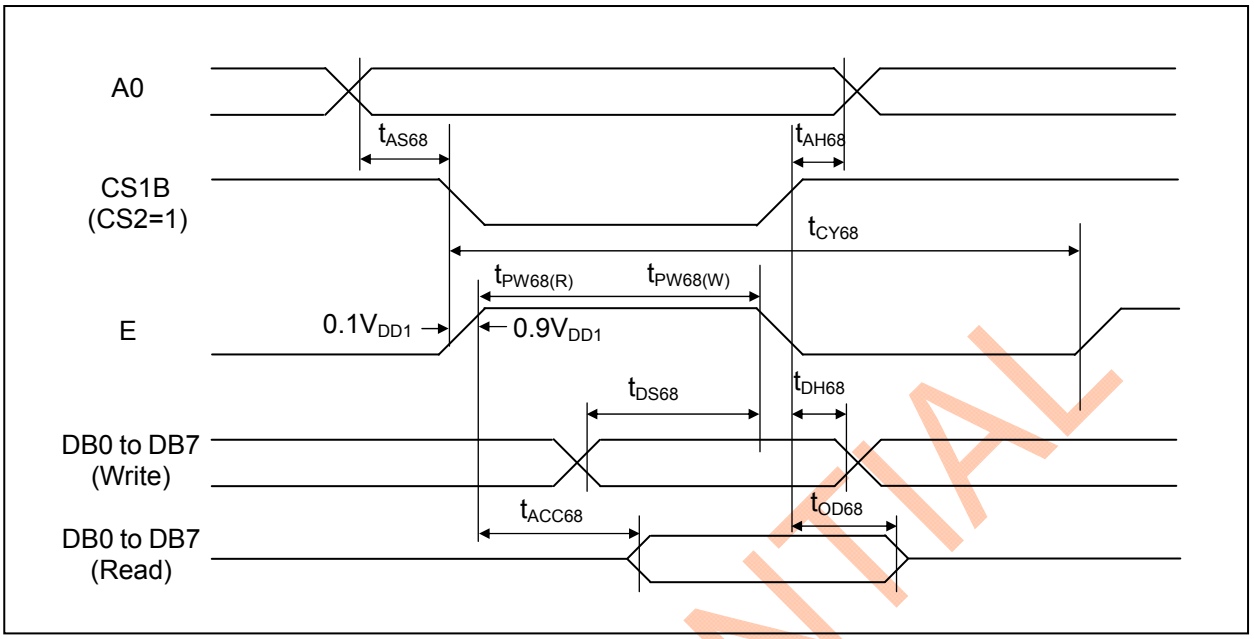
Read / Write Characteristics (8080-series MPU)



(VDD1= 1.8 ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time		$t_{CY80(W)}$	1000	-	-	ns	
		$t_{CY80(R)}$	1500	-	-	ns	
Pulse width (WRB)	RW_WRB	$t_{PW80(W)}$	150	-	-	ns	
Pulse width (RDB)	E_RDB	$t_{PW80(R)}$	500	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	60 0	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	300 -	-	- 10	ns	(No load)

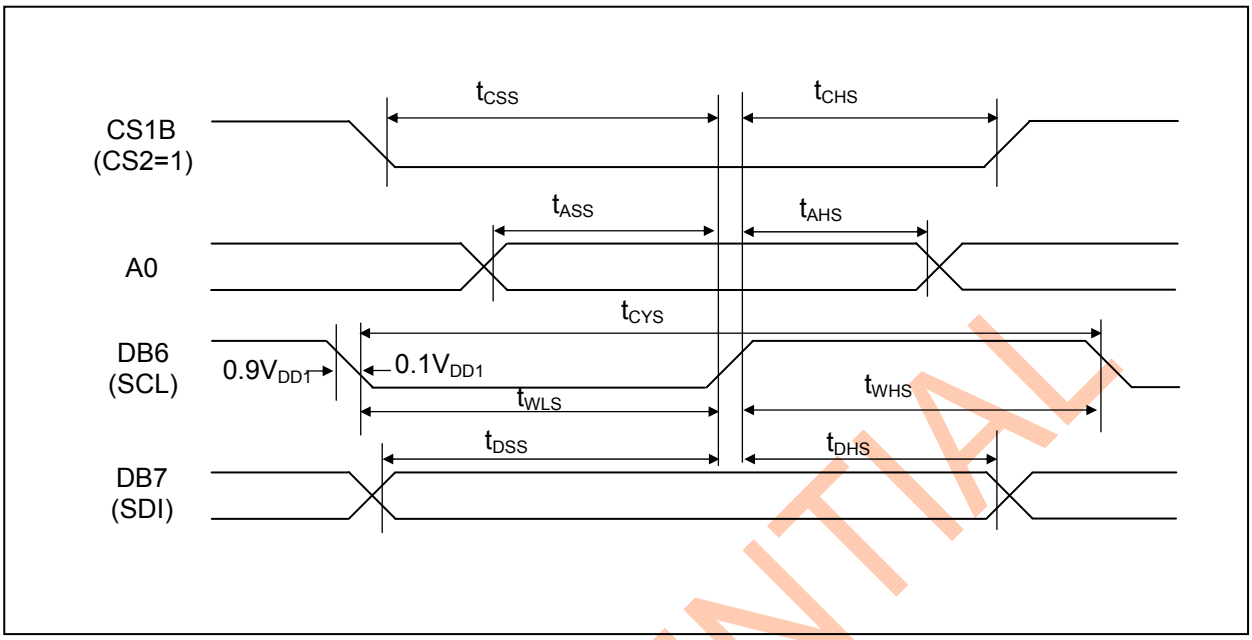
Read / Write Characteristics (6800-series Microprocessor)



(VDD1 = 1.8 ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle time	DB7 to DB0	$t_{CY68(W)}$	1000	-	-	ns	
		$t_{CY68(R)}$	1500	-	-	ns	
Pulse width (E)	RW_WRB	$t_{PW68(W)}$	150	-	-	ns	
Pulse width (E)	E_RDB	$t_{PW68(R)}$	500	-	-	ns	
Data setup time Data hold time		t_{DS68} t_{DH68}	60 0	-	-	ns	
Read access time Output disable time		t_{ACC68} t_{OD68}	300 -	-	- 10	ns	(No load)

Serial Interface Characteristics(SPI3/SPI4)

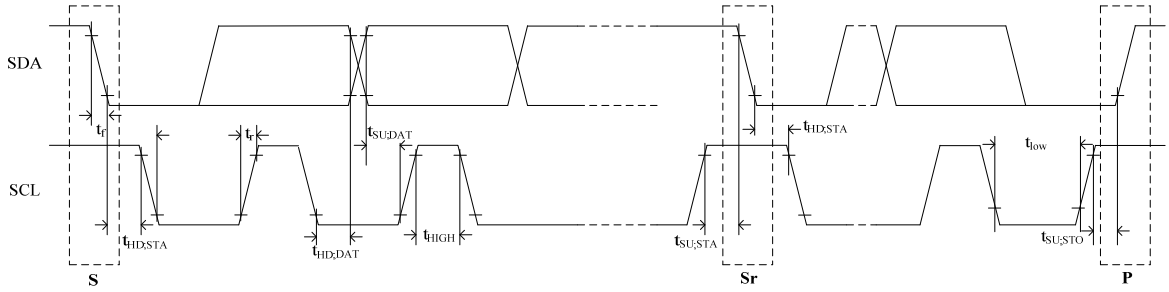


(VDD1 = 1.8 ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB6(SCL) Write	t_{CYS} t_{WHS} t_{WLS}	260 130 100	- - -	- - -	ns	
Serial clock cycle SCL high pulse width SCL low pulse width	DB6(SCL) Read	t_{CYS} t_{WHS} t_{WLS}	700 200 470	- - -	- - -	ns	
Address setup time Address hold time	A0	t_{ASS} t_{AHS}	45 45	- -	- -	ns	
Data setup time Data hold time	DB7 (SDI)	t_{DSS} t_{DHS}	45 45	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	90 90	- -	- -	ns	

Note: All signal Rising time and falling Time <15ns

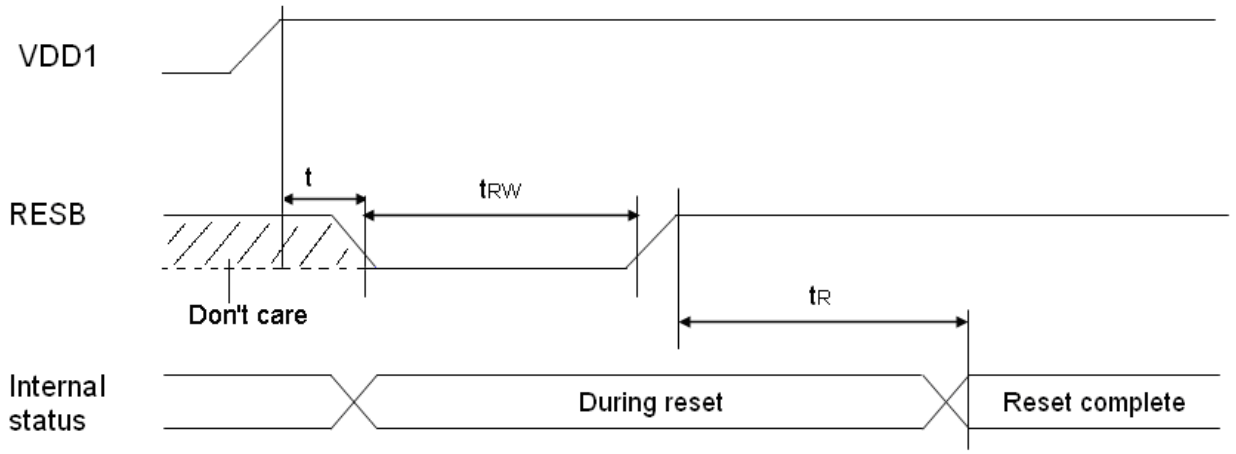
IIC interface Timing Characteristics



(VDD1 = 1.8 ~ 3.6V, Ta = -30 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
SCL clock frequency		fSCL	0	-	400	kHz	
Set-up time for START condition		tSU;STA	600	-	-	ns	
Hold time for START condition		tHD;STA	600	-	-	ns	
Low period of the SCL clock		tLow	1300	-	-	ns	
High period of the SCL clock		tHIGH	600	-	-	ns	
Data set-up time		tSU;DAT	100	-	-	ns	
Data hold time		tHD;DAT	-	-	900	ns	
Rise time of both SDA and SCL signals		tr	-	-	20	ns	
Fall time of both SDA and SCL signals		tf	-	-	20	ns	
Set-up time for STOP condition		tSU;STO	600	-	-	ns	

Reset Input Timing



(VDD1 = 1.8 ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESB	t_{RW}	2	-	-	us	
Reset time	-	t_R	-	-	2	us	
Reset time	RESB	t	0	-	-	us	

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are three modules, PVC generator, VDDL generator and the Multi-level LCD Power Supply divider, and correspondingly controlled by VC, VD[1:0] and VF[1:0] separately.

When the PVC generator is ON (VC="1"), the voltage of PVC is set by RR [7:0]. The boost ratio to be selected is due to the panel load. For better power consumption you should choose the suitable ratio according to the display quality, in the case of sufficient PVC voltage, the smaller boost ratio the higher the efficiency.

When the VDDL generator is ON (VD[1:0]≠"00"), the output voltage of VDDL is set by VD [1:0]. The VDDL should be considered seriously to guarantee the logic function and acquire better consumption performance.

The Multi-level LCD Power Supply divider is controlled by VF[1:0], it is ON when VF[1:0]≠"00". These power supply voltages can be produced in three forms. Trade off should be considered between consumption performance and cost. See details please refer to the Power Supply Configurations.

Power Supply Configurations

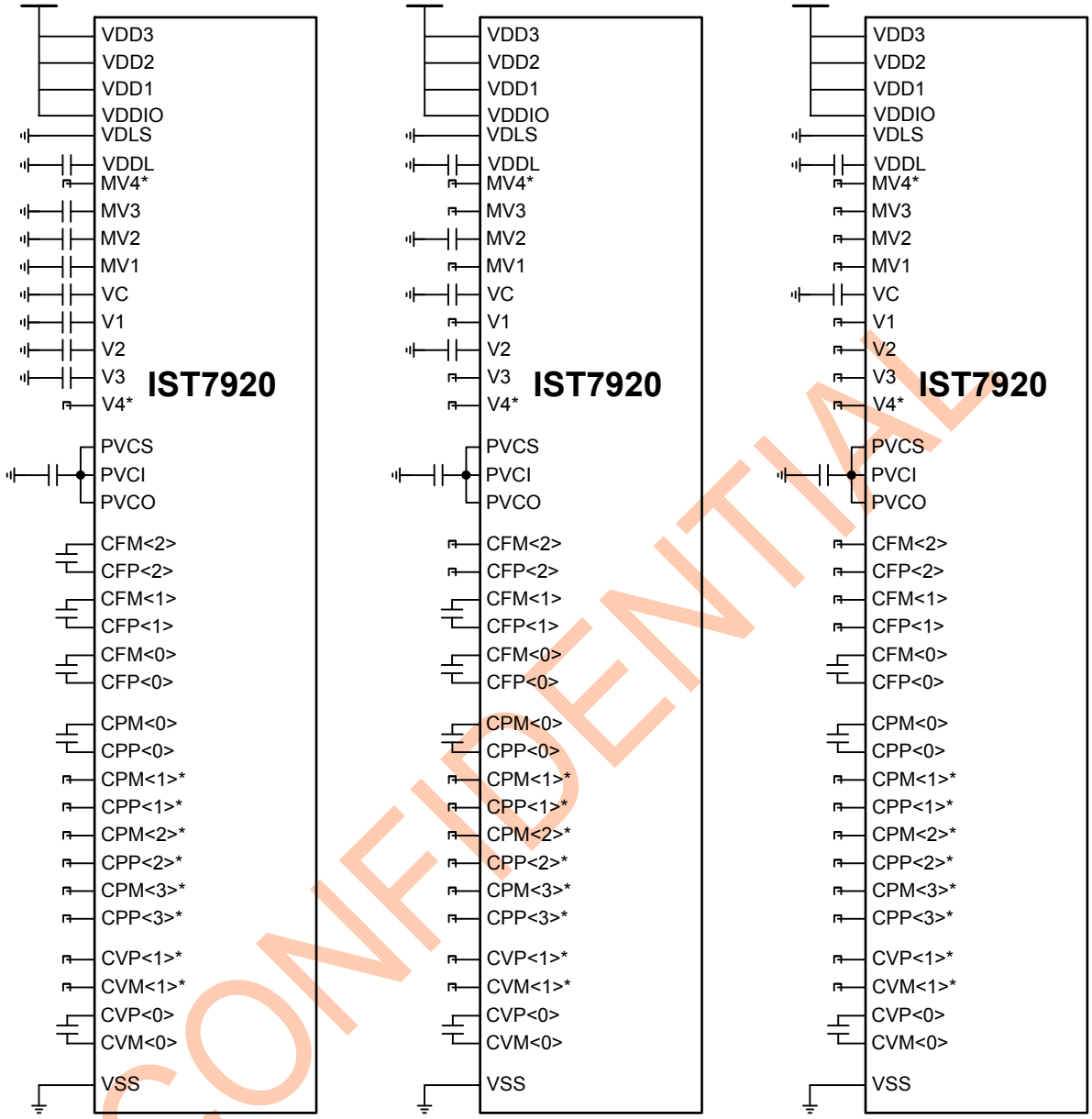
Power Configuration		PVCO/PVCI/PVCS Status
VC	1	Open*1
	0	External input

Power Configuration			VDDL Status		
		VDLS	VDDL Voltages	Caps requirement	Consumption performance
VD[1:0]	00B	1	External input	0	Dependent on applied voltage
	00B	0	VDD1	0	Normal
	01B	VDLS*4	1.8V regulator*2	1(VDDL)	Good
	10B	0	1/2 VDD1*2	1(VDDL) + 1(CV[0])	**Best**
	11B	0	2/3 VDD1*2	1(VDDL) + 2(CV[1:0])	Better

Power Configuration		V4/V3/V2/V1/VC/MV1/MV2/MV3/MV4 Status	
		Caps requirement	Consumption performance
VF[1:0]	00B	0	Dependent on applied voltage
	01B	9(V4~MV4) + 3(CF[2:0])	**Best**
	10B	5(V4/V2/VC/MV2/MV4) + 2(CF[1:0])	Good
	11B	3(V4/VC/MV4) + 1(CF[0])	Better

<Note> *1. PVCO, PVCI and PVCS are short together by ITO and the common node should be connected stabilizing capacitors to VSS;
*2. Stabilizing capacitor should be connected between VDDL and VSS;
*3 NxVDD-0.3<=PVCMAX <= (N+1) xVDD-0.3. N defined by BT1-0:
BT1-0=00, N=2;
BT1-0=01, N=3;
BT1-0=10, N=4;
BT1-0=11, N=5;
*4 First VS=1, VDLS=0, delay more than 10ms then VDLS=1

Power Supply Applications (VDDIO=VDD1=VDD2=VDD3>=2.4V, VDDL=1/2 or 2/3 VDD)



Typical Application A

Configurations:

Power Ctrl (33H) = 2D,

BT = FC (2X), BS (30H) = 00 (1/8).

Typical Application B

Configurations:

Power Ctrl (33H) = 2E,

BT = FC (2X), BS (30H) = 00 (1/8).

Typical Application C

Configurations:

Power Ctrl (33H) = 2F,

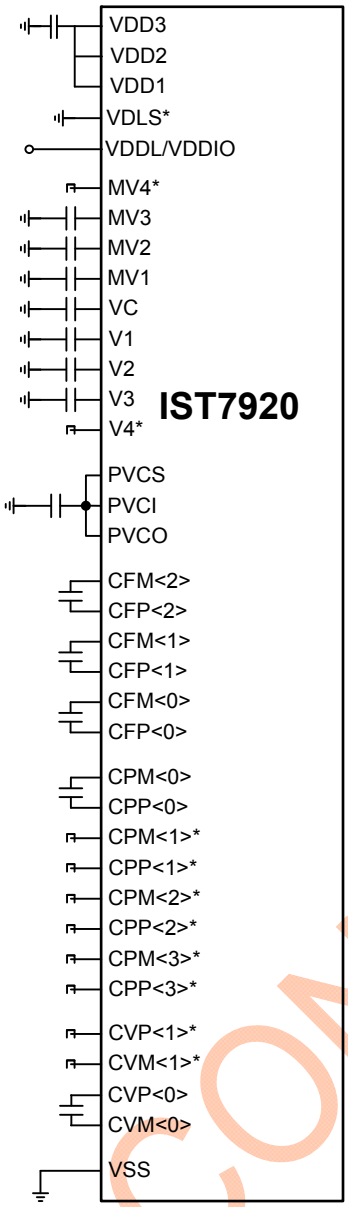
BT = FC (2X), BS (30H) = 00 (1/8).

<Note> 1. The typical value for all capacitors is 0.1μF~10μF, 1μF is recommended if there is no other special noted;

2. If 1/8 BIAS is adopted, stabilizing capacitors for V4 and MV4 is not necessary.
3. The Capacitors between CPP<3:0> and CPM<3:0> are for PVC booster. In 2X mode, the CPX<0> is necessary; 3X mode, the CPX<1:0> is necessary; 4X mode, the CPX<2:0> is necessary; 5X mode, the CPX<3:0> is necessary;
4. When VDDL=1/2VDD is adopted (VD[1:0]=10B), capacitor between CVP<1> and CVM<1> is not necessary;
5. Configurations of VF[1:0] corresponding to different power consumption performance, the performance of the above 3 application circuits is A>B>C.

The application A is recommended for best power consumption performance.
The application C is recommended for least caps and least LCD module cost.

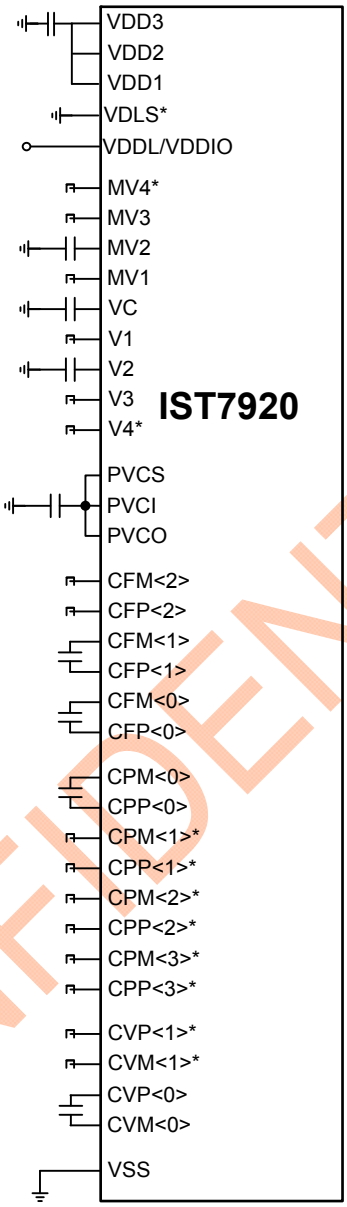
Power Supply Applications (VDDIO=VDDL=1.5~1.8V, VDD1=VDD2=VDD3 connect to 1uF cap)



Typical Application A

Power on sequence:

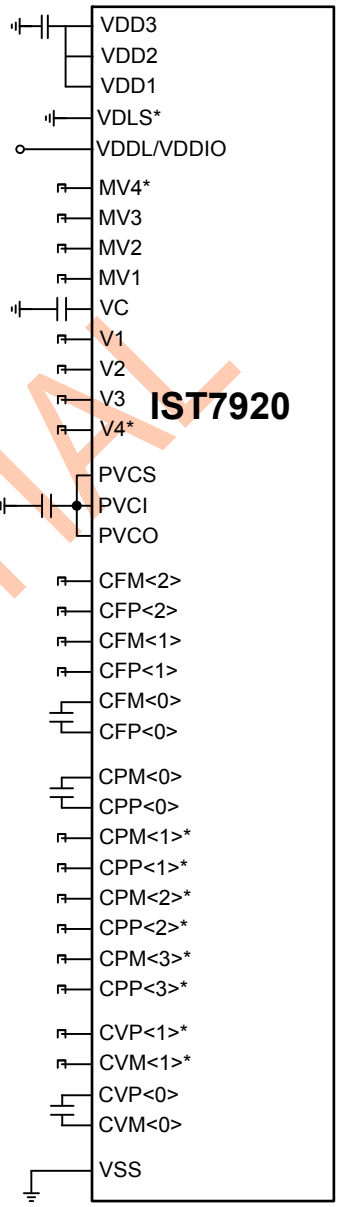
Power Ctrl (33H) = 20H,
Delay 100ms
Power Ctrl (33H) = 2CH,
Delay 300ms
BT = FCH (2X)/FDH (3X),
Delay 100ms
Power Ctrl (33H) = 2DH,
BS (30H) = 00 (1/8).



Typical Application B

Power on sequence:

Power Ctrl (33H) = 20H,
Delay 100ms
Power Ctrl (33H) = 2CH,
Delay 300ms
BT = FCH (2X)/FDH (3X)
Delay 100ms
Power Ctrl (33H) = 2EH,
BS (30H) = 00 (1/8).



Typical Application C

Power on sequence::

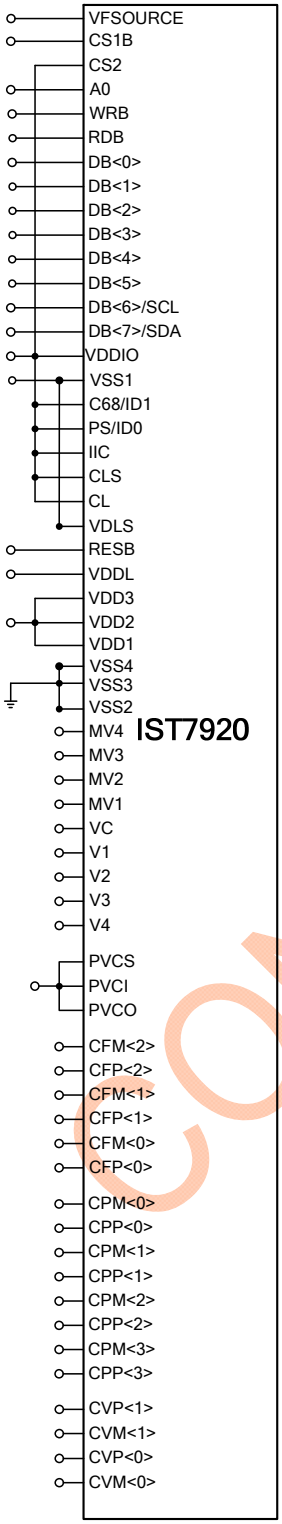
Power Ctrl (33H) = 20H,
Delay 100ms
Power Ctrl (33H) = 2CH,
Delay 300ms
BT = FCH (2X)/FDH (3X)
Delay 100ms
Power Ctrl (33H) = 2FH,
BS (30H) = 00 (1/8).

<Note> 1. The typical value for all capacitors is 0.1μF~10μF, 1μF is recommended if there is no other special noted;
2. If 1/8 BIAS is adopted, stabilizing capacitors for V4 and MV4 is not necessary.
3. The Capacitors between CPP<3:0> and CPM<3:0> are for PVC booster. In 2X mode, the CPX<0> is necessary; 3X mode, the CPX<1:0> is necessary; 4X mode, the CPX<2:0> is necessary; 5X mode, the CPX<3:0> is necessary;
4. When VDD=2xVDDL is adopted (VD[1:0]=10B), capacitor between CVP<1> and CVM<1> is not necessary;
5. Configurations of VF[1:0] corresponding to different power consumption performance, the performance of the above 3 application circuits is A>B>C.

The application A is recommended for best power consumption performance.
The application C is recommended for least caps and least LCD module cost.

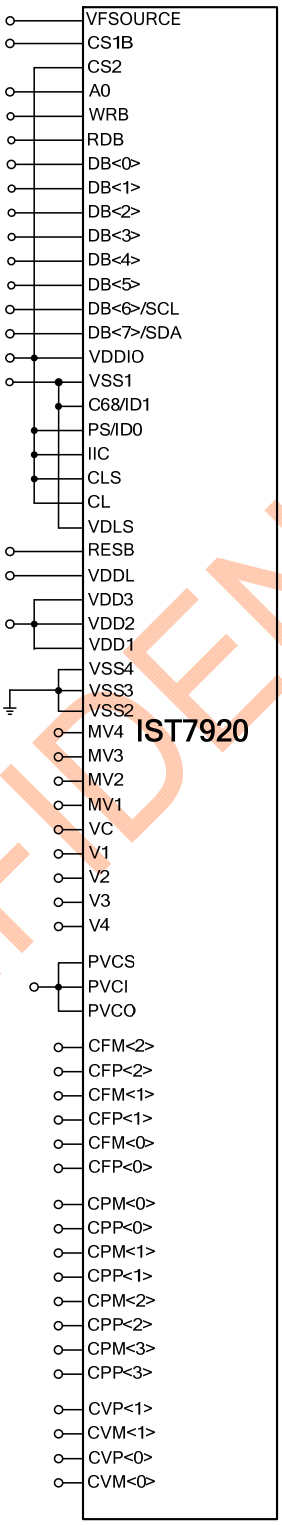
REFERENCE APPLICATIONS

MPU Interface



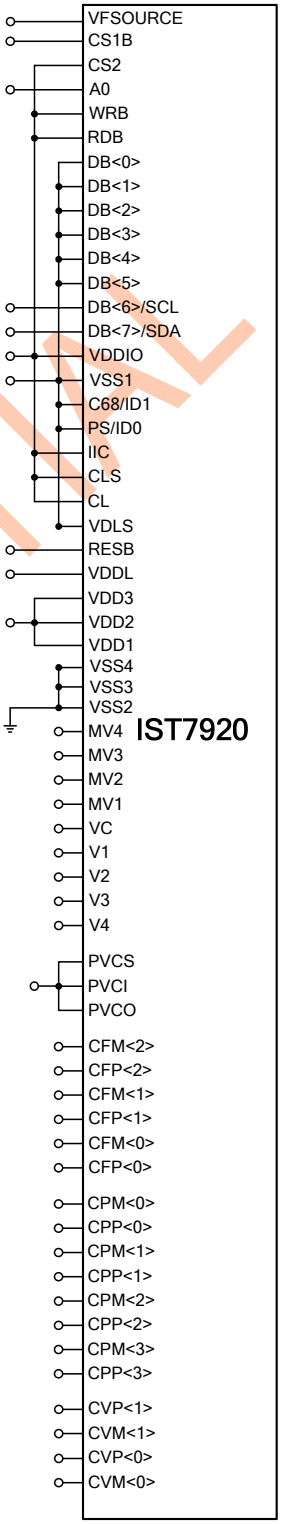
Interface: 6800-series

(C68 = "H", PS = "H", IIC="H")



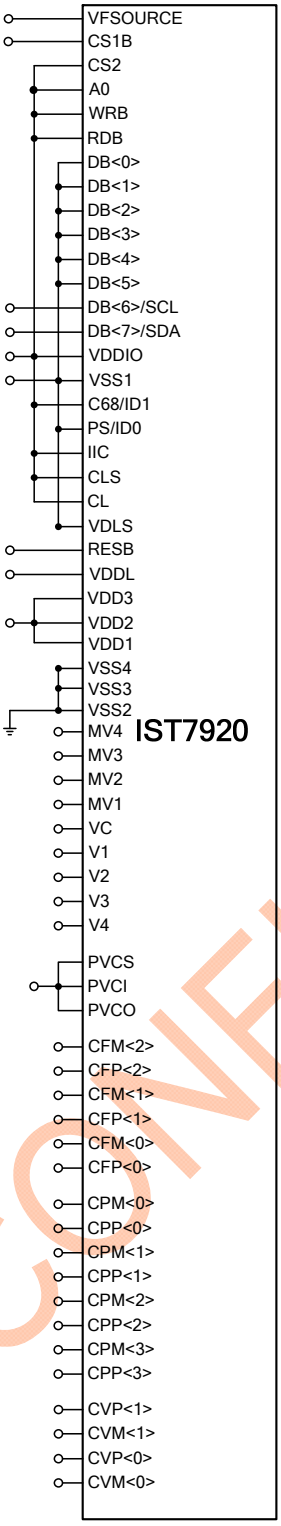
Interface: 8080-series

(C68 = "L", PS = "H", IIC="H")



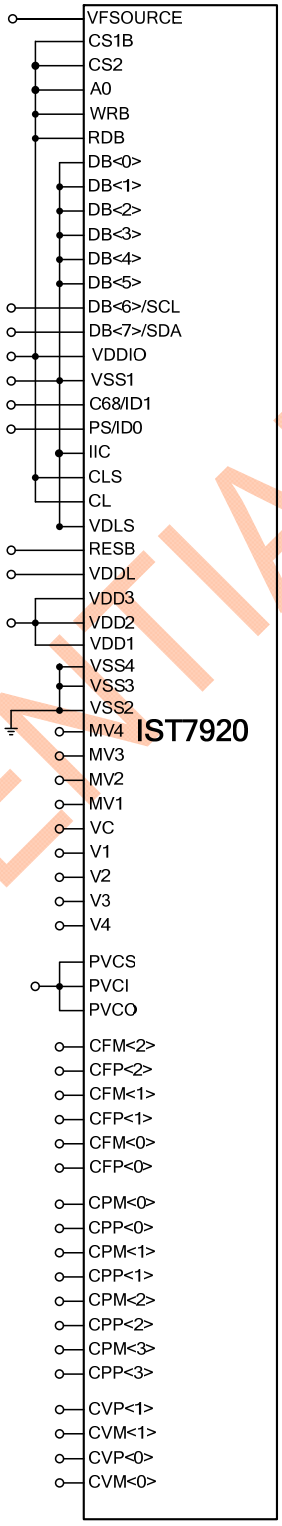
Interface: Serial Interface 4

(C68 = "L", PS = "L", IIC="H")



Interface: Serial Interface 3

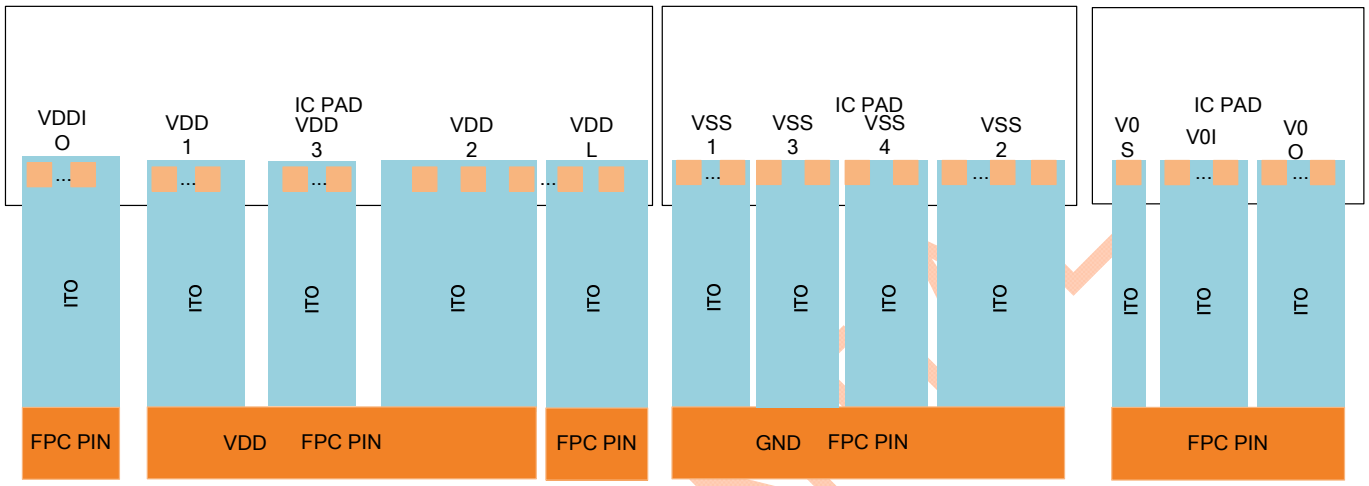
(C68 = "H", PS = "L", IIC="H")



Interface: IIC

(C68 = "ID1", PS = "ID0", IIC="L")

ITO CONNECTION



CAUTIONS:

1. This Specification will be subjected to modify without notice.
2. Precautions on Light:

Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light, therefore, can potentially lead to its malfunctioning.

2.1 Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation.

2.2 Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

2.3 The IC must be shielded from light in the front, back and side faces.

3. ESD control and prevention:

3.1 Humidity Control: 30~70% relative humidity is recommended.

3.2 To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all sources of static fields removed. (Example: Station ionizers).

3.3 Grounding all personnel who come in contact with parts will eliminate a possible source of ESD. (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4. Storage Conditions:

Before open package	After open package
Temp.=25±5℃ Humidity:50~70% Less than 1 Years	Temp.=25±5℃ Humidity:50~70% Less than 3 Months