SURENOO GRAPHIC OLED SERIES DISPLAY

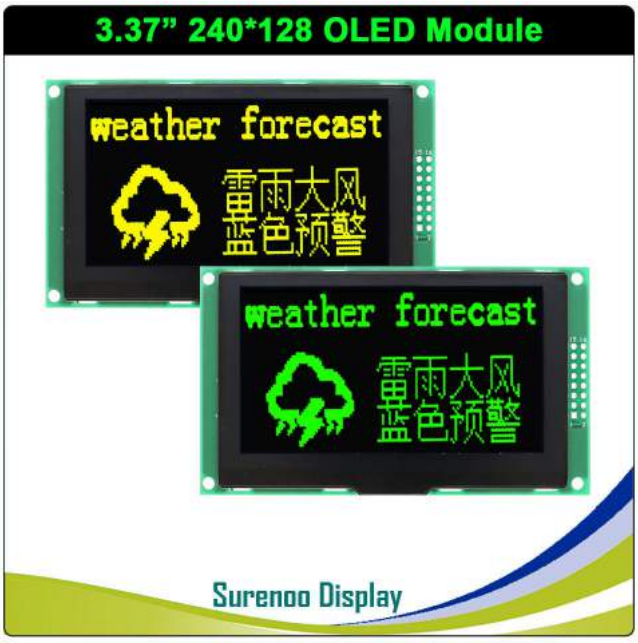
Product Specification

(Preliminary)

Part Name: OEL Display Module

SOG240128A_M337

Please click the following image to buy the sample



Business Card

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Graphic OLED Display Selection Guide

SSD1322

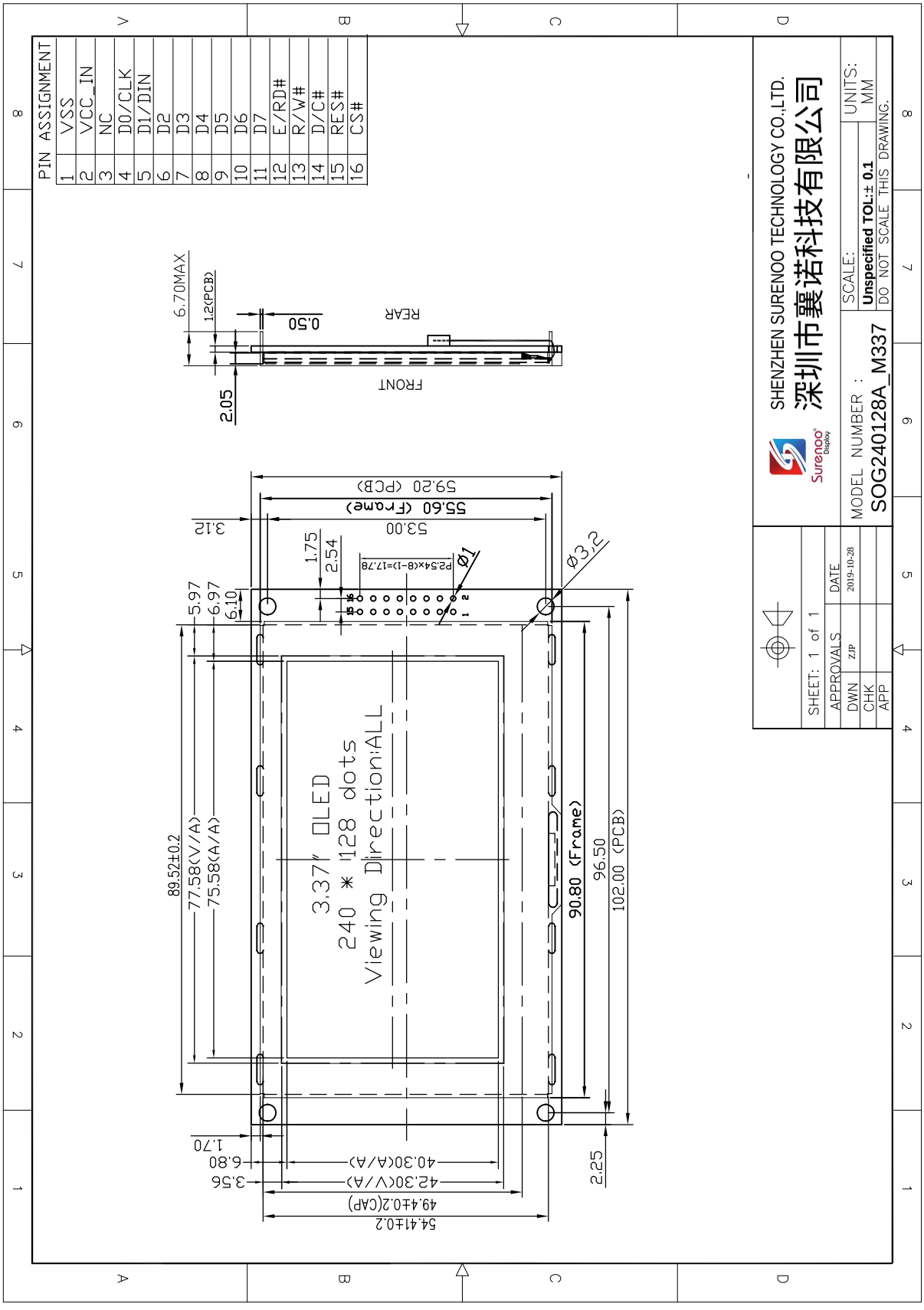
RECORDS OF REVISION

(修订记录)

Part Number (产品型号)	Revision (版本)	Revision Content (修订内容)	Revised on (修订日期)
SOG240128A_M337	V1.0	第一次发行	2019-10-28

CONTENTS

1. Outline Drawing



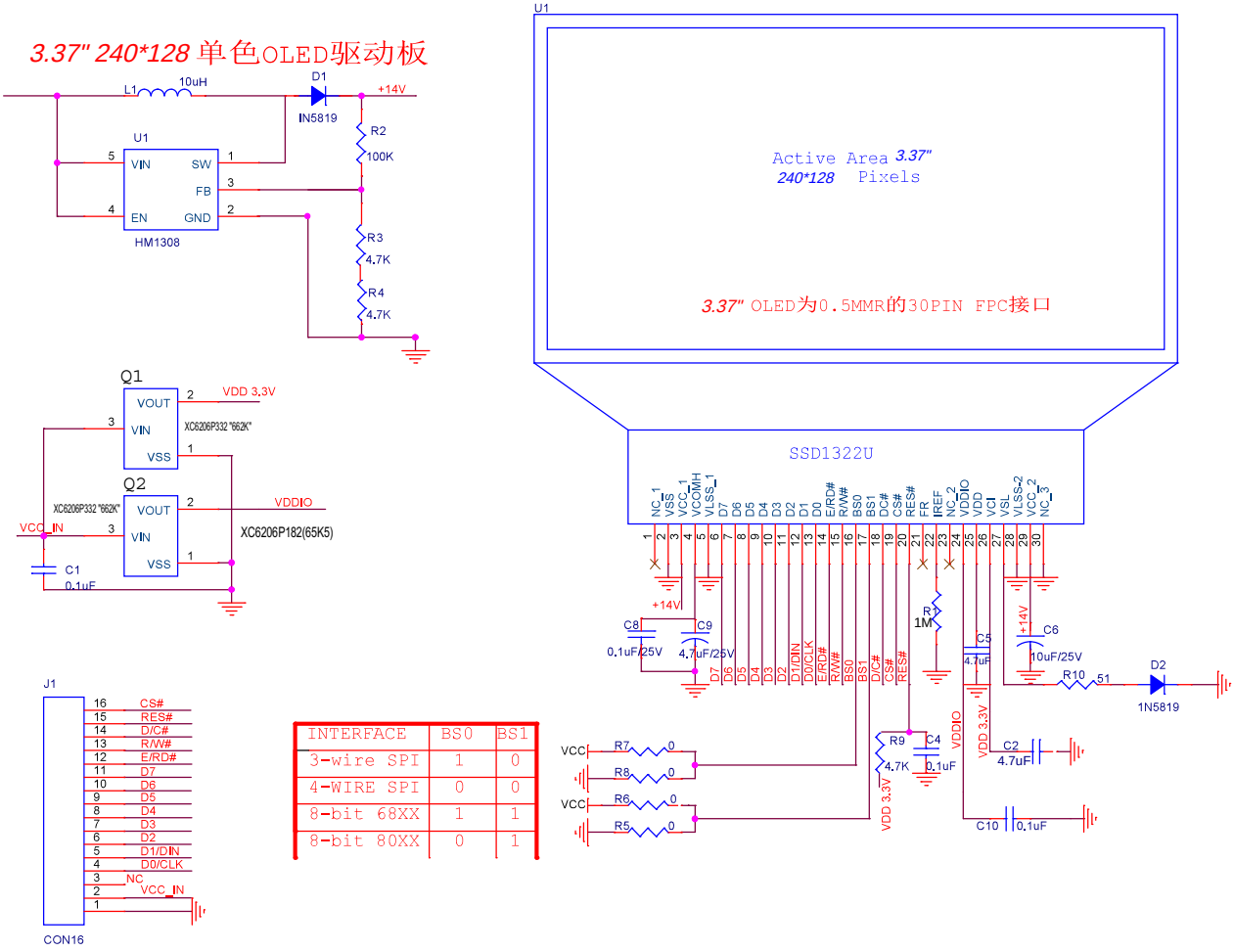
2. Function Characters

2-1. Dots: 240*128 Dots
2-2. Material: PM-OLED
2-3. Color: Yellow / Green
2-4. Gray Scale: 16 Levels
2-5. OLED Module Voltage: 3-5V
2-6. OLED Panel Drive Voltage: 14.0V
2-7. Operate Temperature: -30~80°C
2-8. Storage Temperature: -40~85°C
2-9. Controller: SSD1322 (30P/0.5)
2-10. Interface: 6800 /8080 /3-4 Wire SPI
2-11. View Angle: All

3. Mechanical specifications

3-1. Model Size: 102.00(L)*59.20(W)*6.70(T) MM
3-2. View Area: 77.58(L)*42.30(W) MM
3-3. Active Area: 75.58(L)*42.30(W) MM
3-4. Dot Size: 0.290*0.290MM
3-5. Dot Pitch: 0.315*0.315MM

4. Block Diagram



5. PIN Description

Pin No.	Symbol	Function
1	GND	Ground.
2	VCC_IN	Power supply pin for core logic operation.
3	NC	No connect
4	D0/CLK	Data Bus / Clock (SPI)
5	D1/DIN	Data Bus / Data (SPI)
6	D2	Data Bus
7	D3	Data Bus
8	D4	Data Bus
9	D5	Data Bus
10	D6	Data Bus
11	D7	Data Bus
12	E/RD#	Enable Signal
13	R/W#	H: Read, L: Write
14	D/C#	H: Data, L: Command
15	RES#	Active LOW Reset signal.
16	CS#	Chip Select

6. ELECTRO-OPTICAL CHARACTERISTICS

6-1 DC ELECTRO-OPTICAL CHARACTERISTICS

DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 3	11.5	12	12.5	V
High Level Input	V_{IH}		$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2 \times V_{DDIO}$	V
High Level Output	V_{OH}	I_{out} = 100μA, 3.3MHz	$0.9 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{out} = 100μA, 3.3MHz	0	-	$0.1 \times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	26.3	32.9	mA
		Note 5	-	41.1	51.4	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{CI} = 2.8V, V_{CC} = 12V, 50% Display Area Turn on.
Note 5: V_{CI} = 2.8V, V_{CC} = 12V, 100% Display Area Turn on.

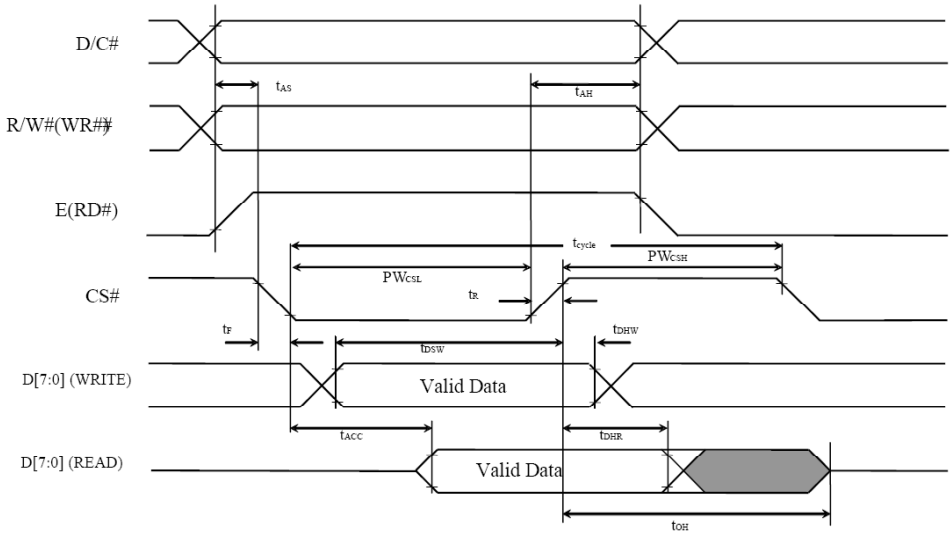
* Software configuration follows Section 4.4 Initialization.

6-2 AC ELECTRO-OPTICAL CHARACTERISTICS

6-2.1、68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



6-2.2、 80XX-Series MPU Parallel Interface Timing Characteristics:

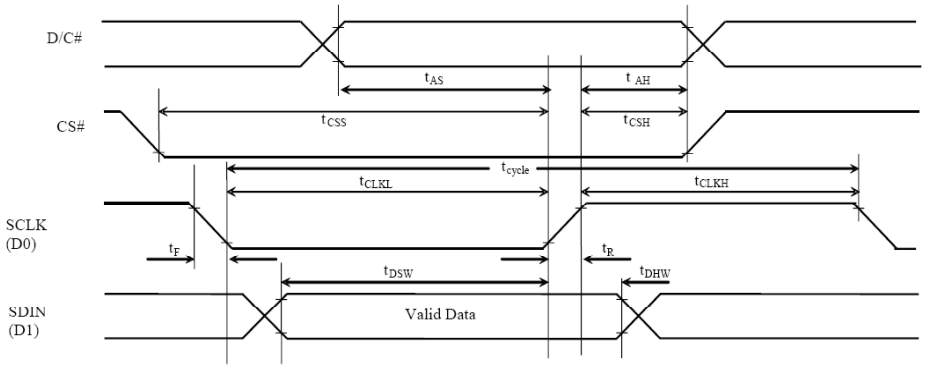
Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

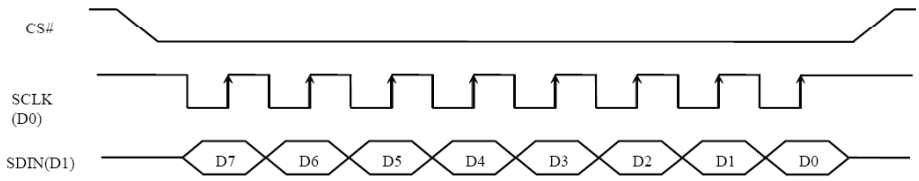
* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

6-2.3、 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

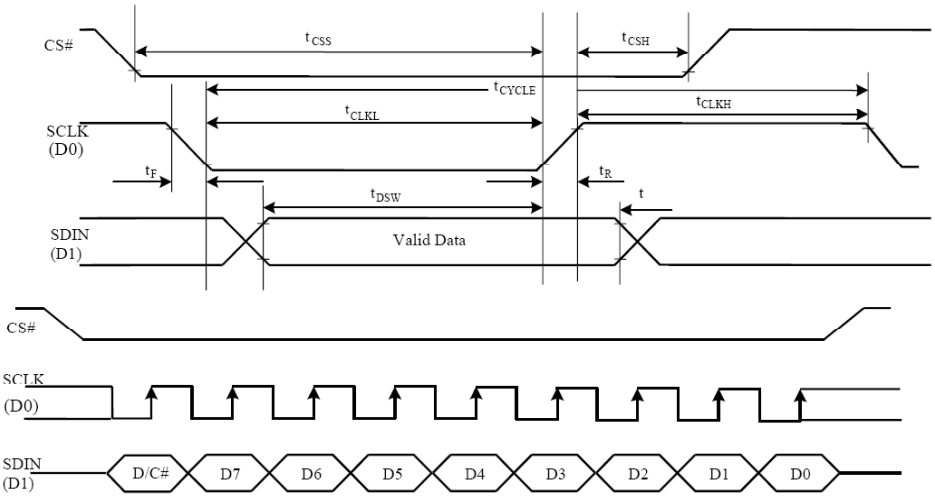




6-2.4、 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



7. Instruction Table

COMMAND TABLE

(D/C#=0, R/W#(WR#) = 0, E(RD#)=1) unless specific setting is stated)

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A_5 0	0 A_4 B_4	0 0 0	0 A_2 0	0 A_1 0	0 A_0 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N 1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 00b, Disable Dual COM mode [reset] 01b, Enable Dual COM mode (MUX ≤ 63) **Note** (1) COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by COM from 0-127 The value is reset to 00H after RESET
0	A4~A7	1	0	1	0	0	X	X_1	X_0	Set Display Mode	A4h = Entire Display OFF, all pixels turns OFF in GS level 0 A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Normal Display [reset] A7h = Inverse Display (GS0ÆGS15, GS1ÆGS14, GS2ÆGS13, …)
0 1 1	A8 A[6:0] B[6:0]	1 0 0	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	1 A_3 B_3	0 A_2 B_2	0 A_1 B_1	0 A_0 B_0	Enable Partial Display	This command turns ON partial mode. The partial mode display area is defined by the following two parameters, A[6:0]: Address of start row in the display area B[6:0]: Address of end row in the display area, where B[6:0] must beA[6:0]
0	A9	1	0	1	0	1	0	0	1	Exit Partial Display	This command is sent to exit the Partial Display mode
0 1	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A	Function Selection	A[0]=0b, Select external V_{DD} A[0]=1b, Enable internal V_{DD} regulator [reset]
0	AE~AF	1	0	1	0	1	1	1	X	Set Sleep mode ON/OFF	AEh = Sleep mode ON (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow: A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow:

A[3:0]	Phase 1 period
0000	invalid
0001	invalid
0010	5 DCLKs
0011	7 DCLKs
0100	9 DCLKs [reset]
:	:
1111	31 DCLKs

A[7:4]	Phase 2 period
0000	invalid
0001	invalid
0010	invalid
0011	3 DCLKs
:	:
0111	7 DCLKs [reset]
:	:
1111	15 DCLKs

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B3	1	0	1	1	0	0	1	1	Set Front Clock Divider / Oscillator Frequency	A[3:0] [reset=0], divide by DIVSET where A[7:4] Oscillator frequency, frequency increases as level increases [reset=1100b]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B5	1	0	1	1	0	1	0	1	Set GPIO	A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH A[3:2] GPIO1:00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	B6	1	0	1	1	0	1	1	0	Set Second Precharge Period	A[3:0] Second Pre-charge period 0000b 0 dclk 0001b 1 dclk …… 1000b 8 dclks [reset] …… 1111b 15 dclks
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A14[7:0]: Gamma Setting for GS14, A15[7:0]: Gamma Setting for GS15 Note (1) 0 Setting of GS1 < Setting of GS2 < Setting of GS3 < Setting of GS14 < Setting of GS15 Refer to Section 8.8 for details (2) The setting must be followed by the Enable Gray Scale Table command (00h)
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A14[7:0]	$A14_7$	$A14_6$	$A14_5$	$A14_4$	$A14_3$	$A14_2$	$A14_1$	$A14_0$		
1	A15[7:0]	$A15_7$	$A15_6$	$A15_5$	$A15_4$	$A15_3$	$A15_2$	$A15_1$	$A15_0$		

A[3:0]	DIVSET
0000	divide by 1
0001	divide by 2
0010	divide by 4
0011	divide by 8
0100	divide by 16
0101	divide by 32
0110	divide by 64
0111	divide by 128
1000	divide by 256
1001	divide by 512
1010	divide by 1024
>=1011	invalid

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B9	1	0	1	1	1	0	0	1	Select Default Linear Gray Scale table	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 8; GS3 level pulse width = 16; : : GS14 level pulse width = 104; GS15 level pulse width = 112 Refer to Section 8.8 for details
0 1	BB A[4:0]	1 *	0 *	1 *	1 A_4	1 A_3	0 A_2	1 A_1	1 A_0	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h] A[5:1] / Hex code / pre-charge voltage 00000 / 00h / 0.20 x V_{CC} : / : / : 11111 / 3Eh / 0.60 x V_{CC}
0 1	BE A[3:0]	1 *	0 *	1 *	1 *	1 A_3	1 A_2	1 A_1	0 A_0	Set V_{COMH}	Set COM deselect voltage level [reset = 04h] A[3:0] = A[2:0] / Hex code / V_{COMH} 0000 / 00h / 0.72 x V_{CC} : / : / : 0100 / 04h / 0.80 x V_{CC} : / : / : 0111 / 07h / 0.86 x V_{CC}
0 1	C1 A[7:0]	1 A_7	1 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Current	A[7:0]: Contrast current value, range:00h~FFh, i.e. 256 steps for I_{SEG} current [reset = 7Fh]
0 1	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Contrast Current Control	A[3:0] = 0000b, reduce output currents for all colors to 1/16 0001b, reduce output currents for all colors to 2/16 : 1110b, reduce output currents for all colors to 15/16 1111b, no change [reset]
0 1	CA A[6:0]	1 *	1 A_6	0 A_5	0 A_4	1 A_3	0 A_2	1 A_1	0 A_0	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX A[6:0] = 15d represents 16MUX : A[6:0] = 127d represents 128MUX [reset]
0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

Note
(1) "*" stands for "Don't care".